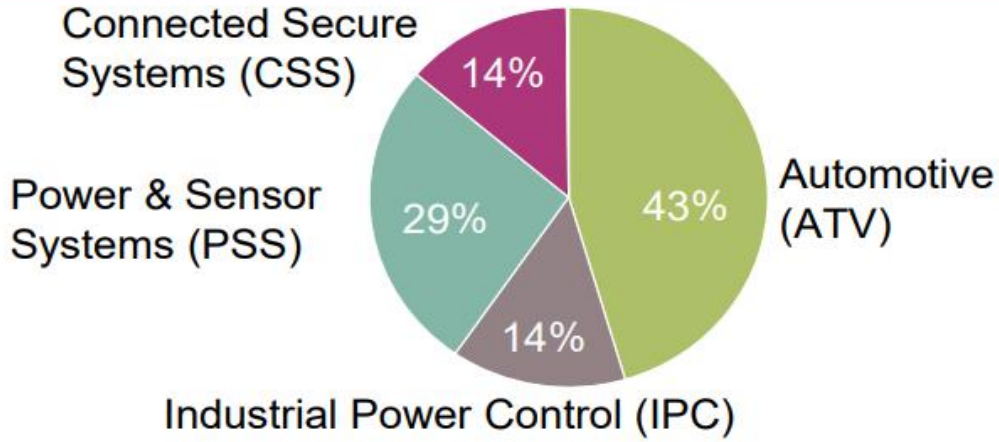
Wide Band Gap devices for EV charging power stack design

Pradip Chatterjee, Infineon Technologies,
Principal Engineer and System Architect

Infineon at a glance

Business Segments Revenue*



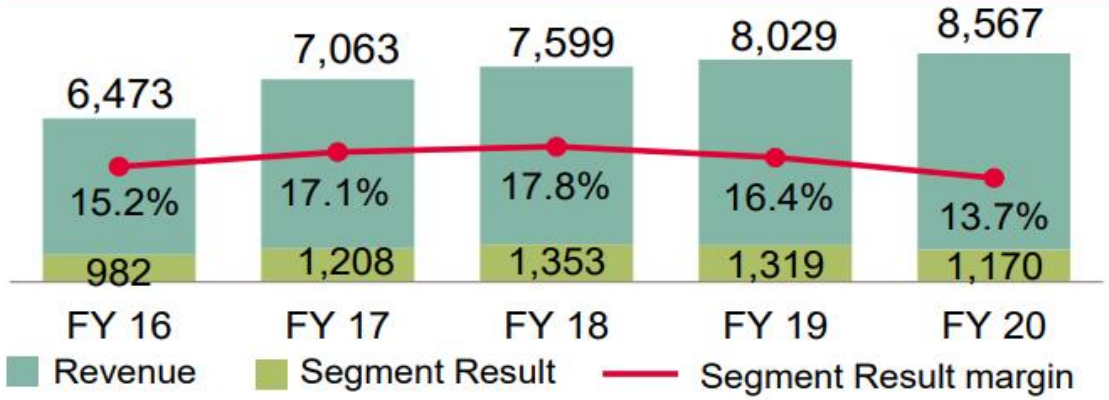
Employees*

46,700 employees worldwide

60 R&D locations

19 manufacturing locations**

Financials



*2020 Fiscal Year (as of 30 September 2020)

**as of 1 April 2021

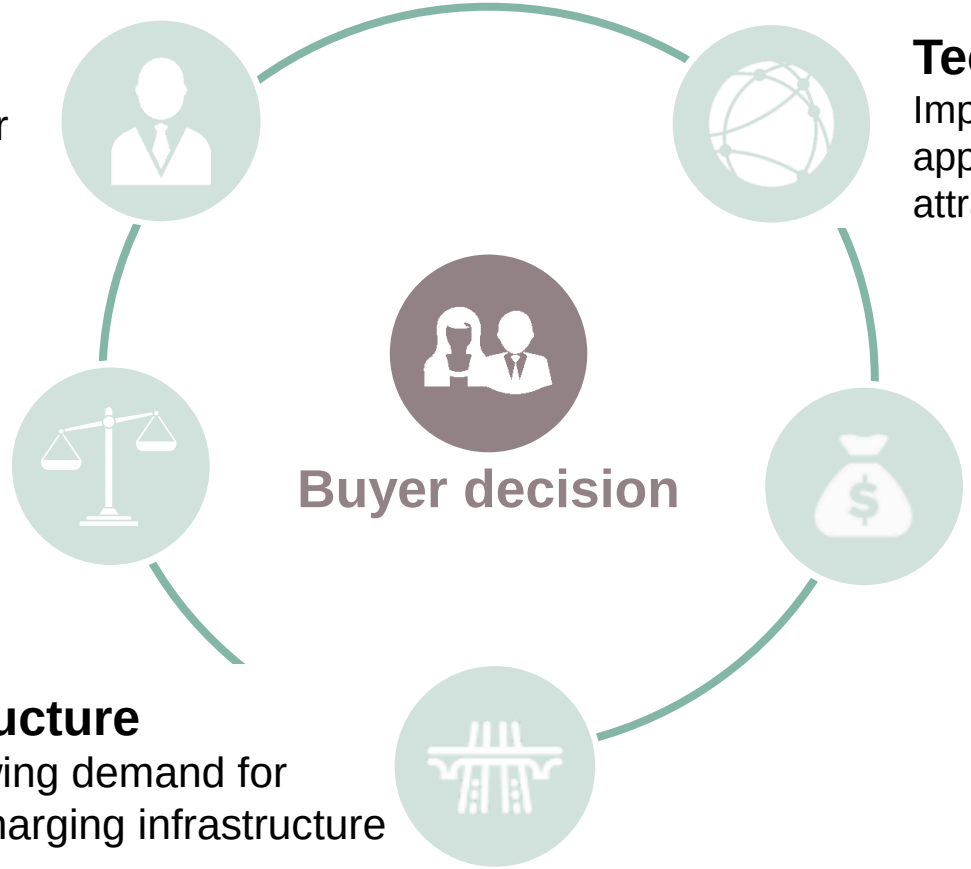
Market Position

Automotive	Power	Microcontroller
		
# 1	**# 1**	**# 3**
Strategy Analytics, April 2021	Omdia, September 2020	Omdia, March 2021

For further information: Infineon Annual Report 2020

Electro-mobility market - key influence factors

To **increase sustainability, electrification of mobility** is inevitable – in both, **private and public** transport segment



OEMs strategies
Fast growing demand for electric vehicles

Technologies
Improvements in technologies and better application knowledge increase attractiveness of e-Mobility

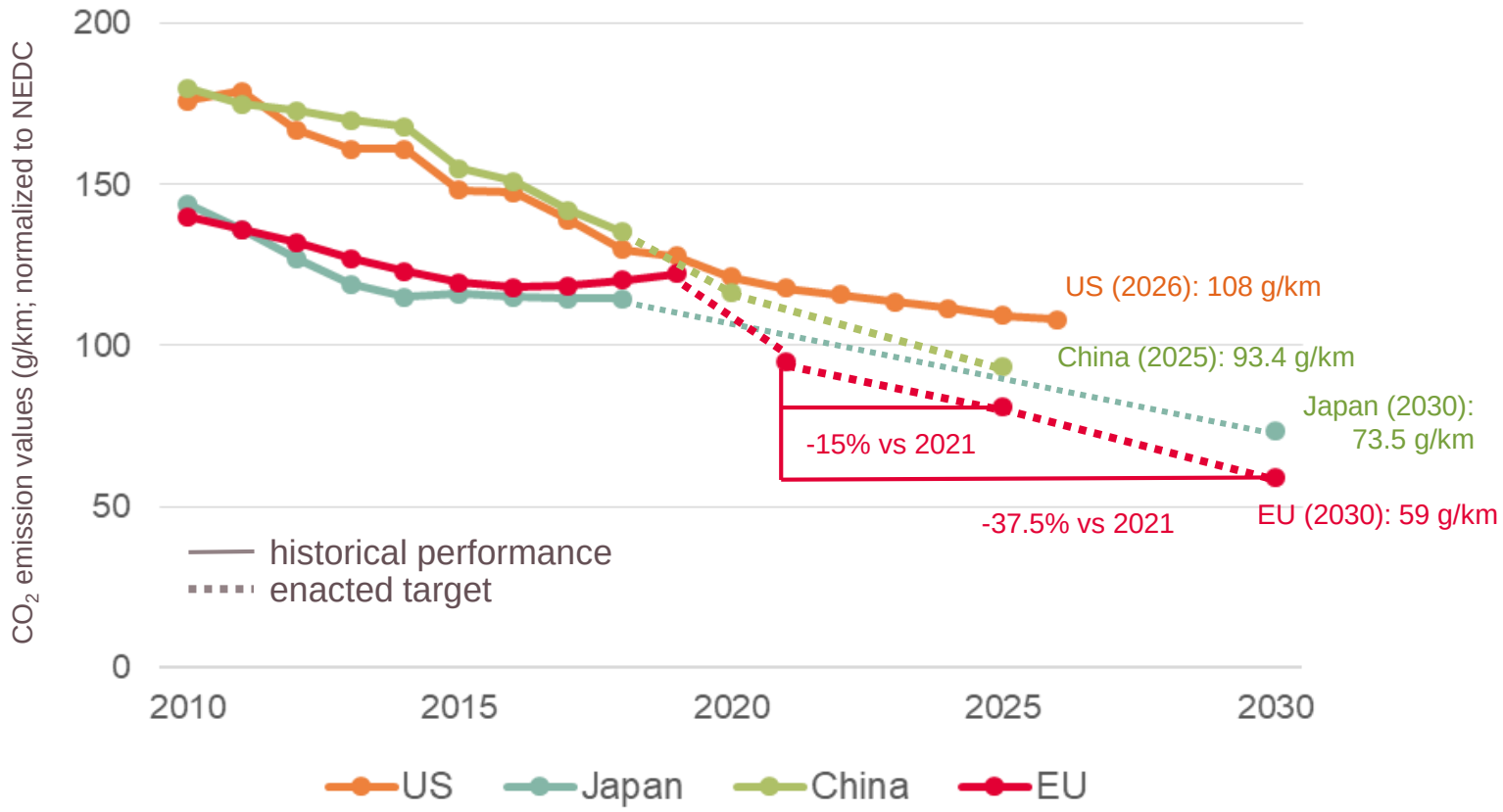
Regulations
Government regulations on CO_2 emissions

Costs
Continuous decrease in battery costs

Infrastructure
Fast growing demand for electric charging infrastructure

The EV market is witnessing strong growth driven by more stringent legal guidelines, demanding significant infrastructure investment

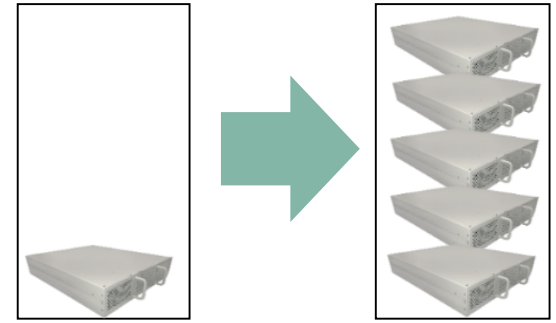
Passenger car CO_2 emission development and regional regulations



Source: The International Council on Clean Transportation (ICCT): *Passenger vehicle fuel economy.* May 2020.

Growing penetration of electro-mobility will drive roll-out of DC charging infrastructure

DC charging system			Charging time**
DC wall box and subunit* Uni- and bi-directional topologies	20 kW (2 subunit of 10 kW)	DC	120 min
Commercial high power charger Single unit and modular subunit designs	50 kW (3 subunits of 20 kW each)	DC	48 min
	150 kW (5 subunits of 30 kW each)	DC	16 min
Hyper fast charger Single unit and modular subunit designs	350 kW (6 subunits of 60 kW each)	DC	7 min



30 kW 150 kW

*) Subunit: A power electronic arrangement build from both active and passive components to convert AC input to dedicated DC output. Often referred to as "module".

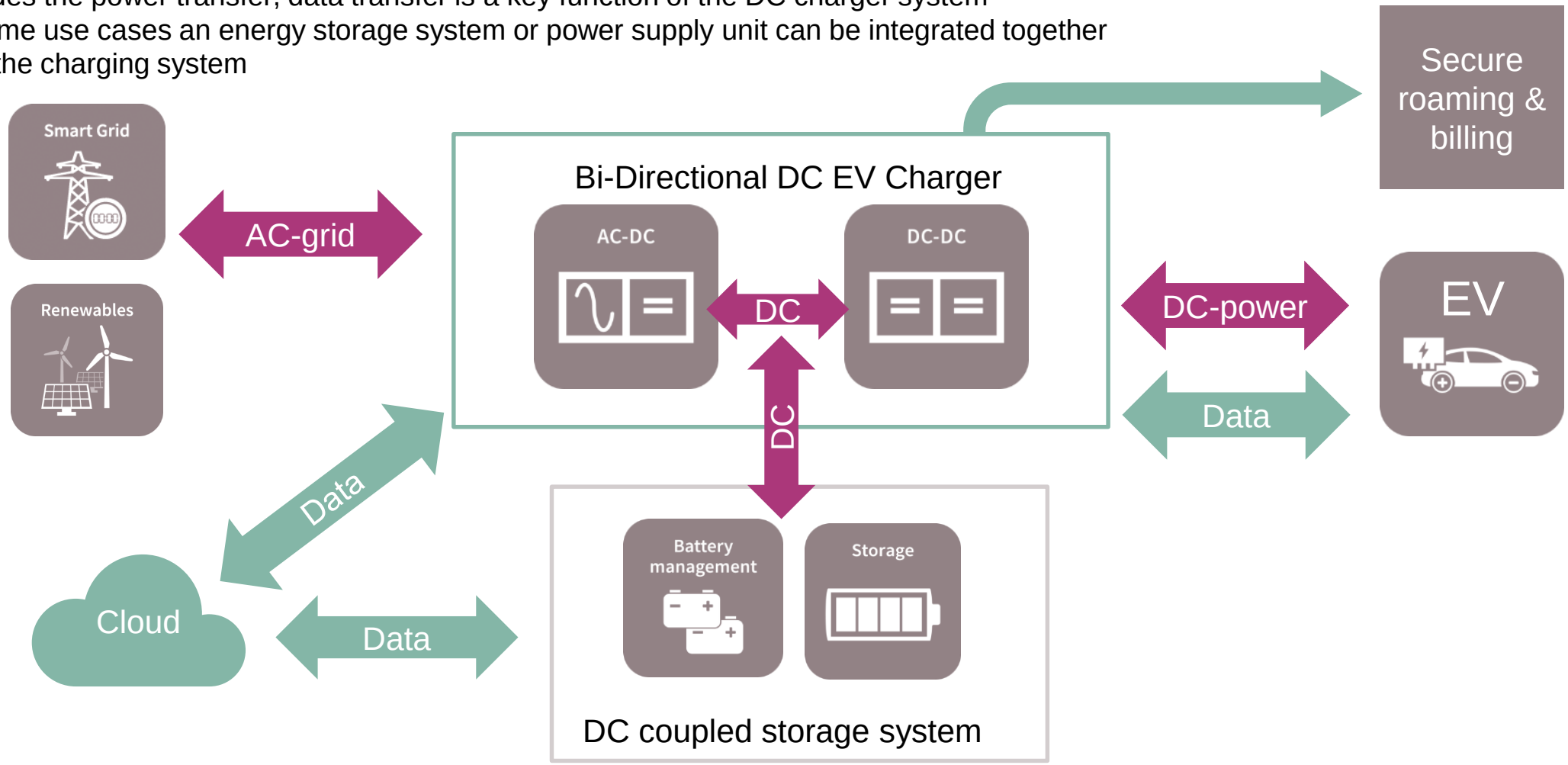
**) Charging time for 200 km

DC EV charging applications – system requirements for the application

- **Battery charging** is a mostly **constant current** application with **typically low demand in dynamics**
- Thermal cycling 10,000 – 30,000 cycles/year
- 15 – 20 years of service
- Ultra-high-power charging > 350 kW
  - Up to 1000 V_{DC} and up to 500 A
- Wide variation of DC output voltage
  - 200 V to 920 V
- **Efficiency** target **98%** (currently 95%)

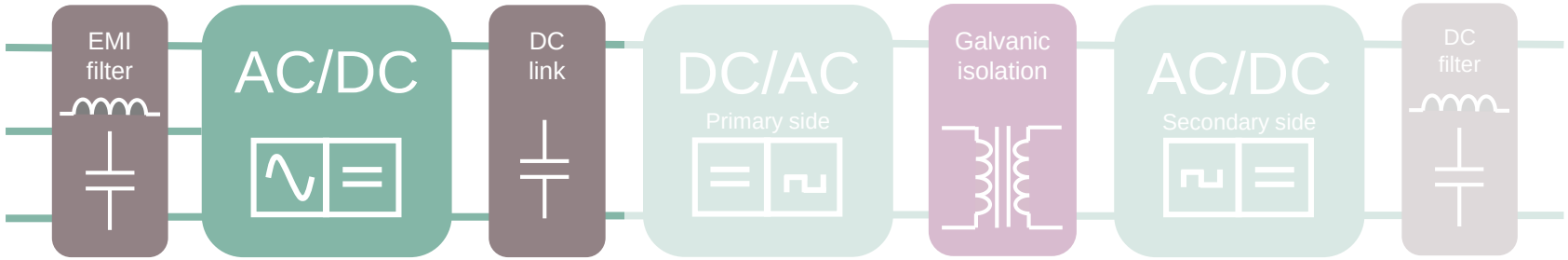
DC EV charger as a key interface between grid, car and digital processes

- Besides the power transfer, data transfer is a key function of the DC charger system
- In some use cases an energy storage system or power supply unit can be integrated together with the charging system

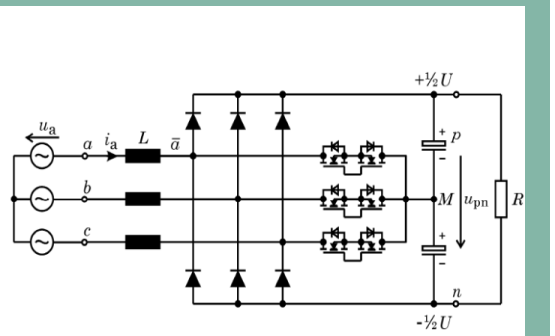


Commonly used topologies for AC/DC conversion

Rectifiers exist in different forms and types

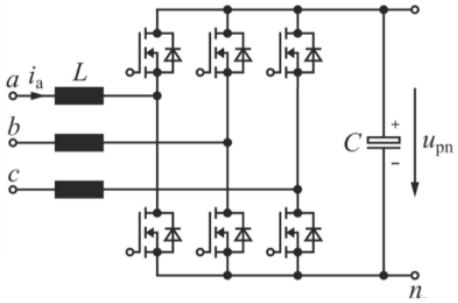


< 50 kW design



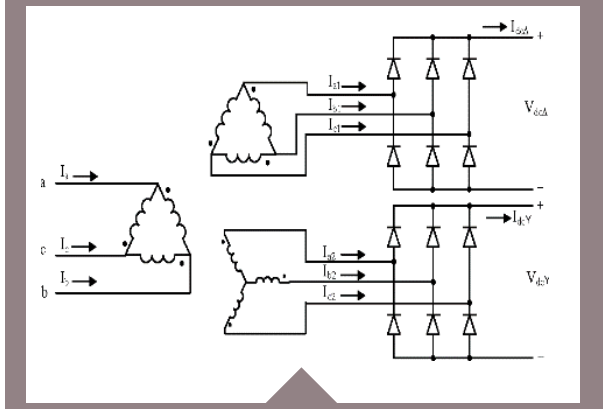
Vienna rectifier

> 50 kW design



Active front end

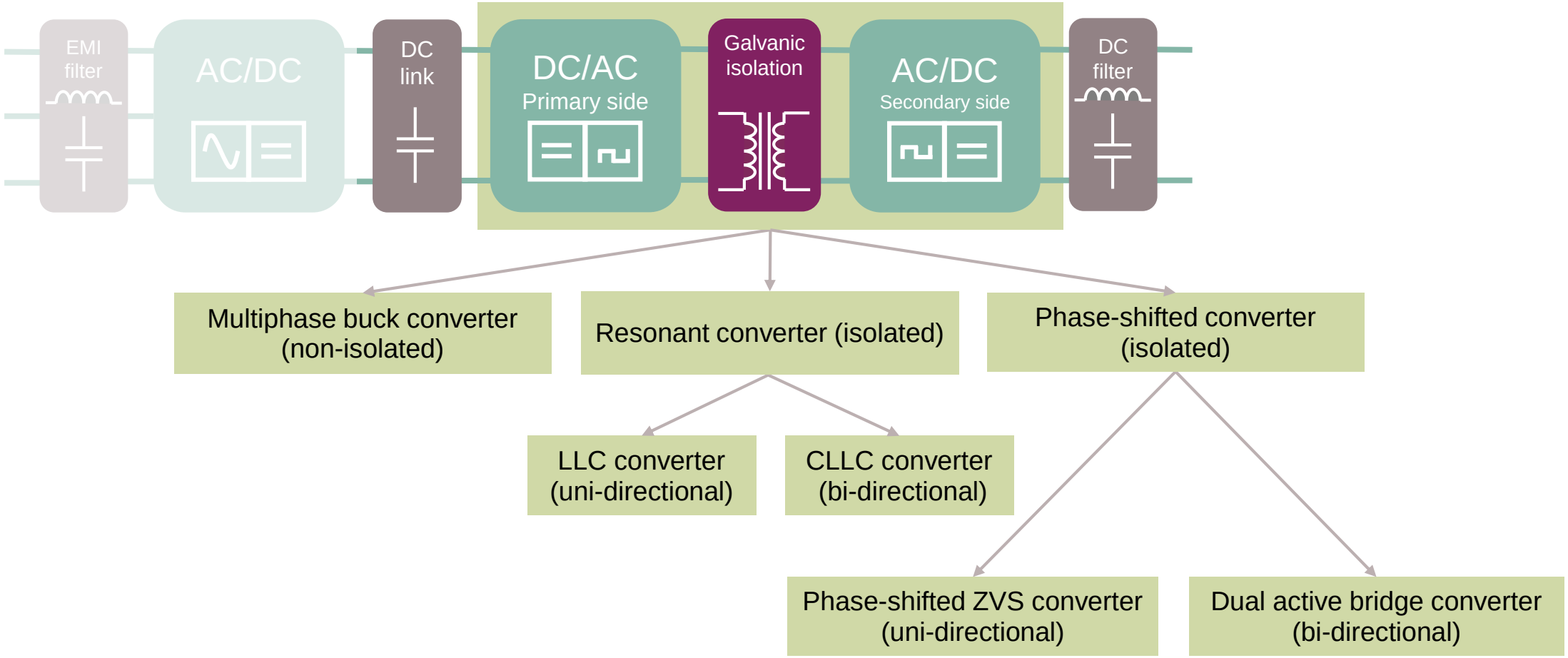
> 100 kW design



Diode rectifier

DC/DC power conversion topologies

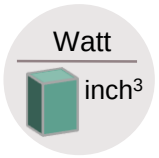
DC-DC converter also exist in different types



System Optimization: A tricky balance to achieve

For power electronics…

Does efficiency matter? — **YES**

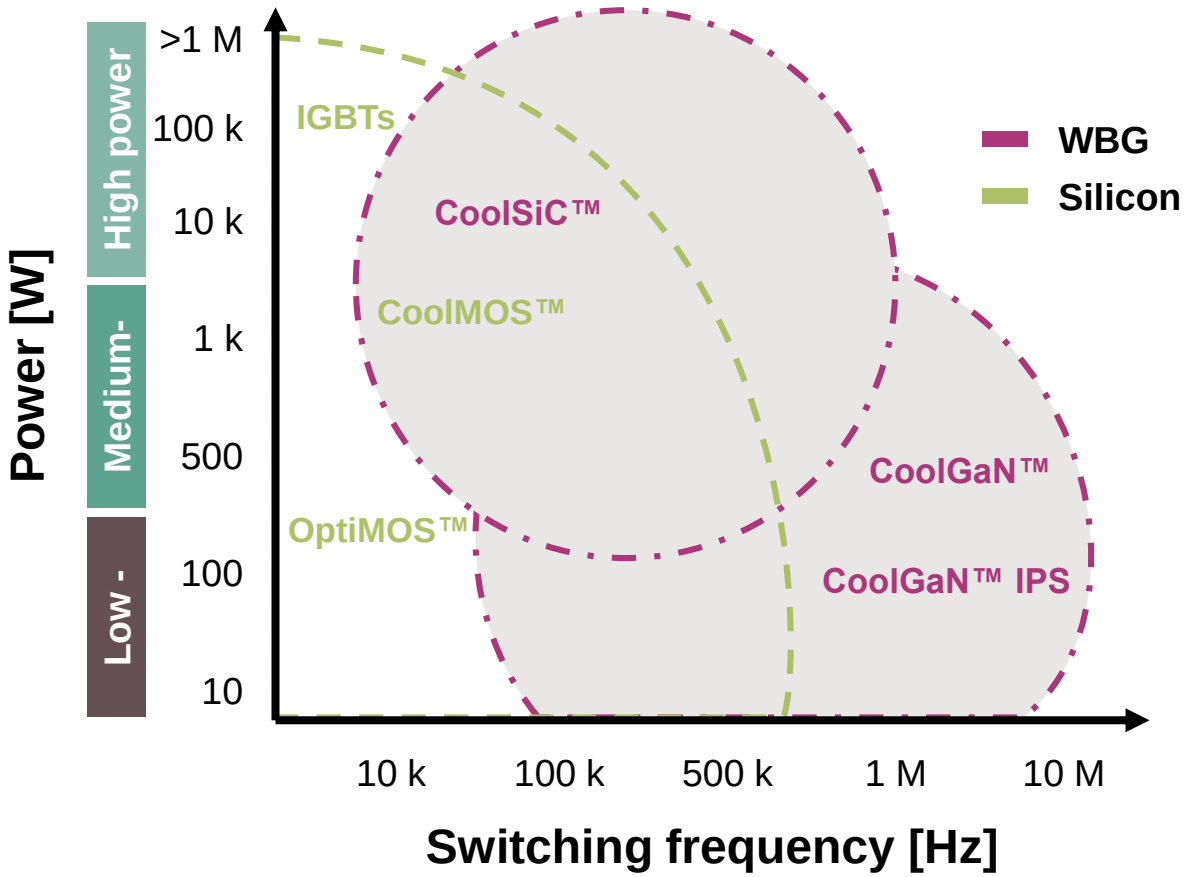


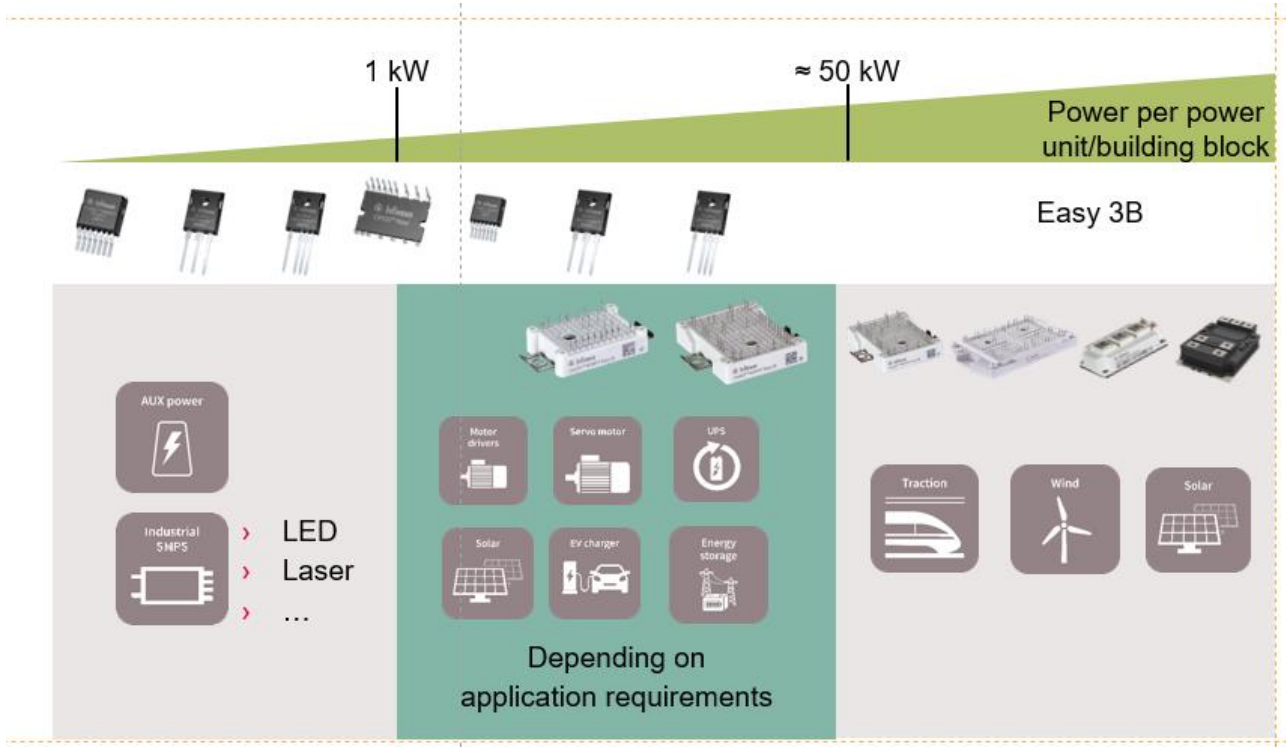
Does power density matter? — **YES**

Is power density achievable only with higher switching frequency? — **YES & NO**

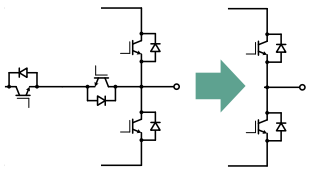
Industrial design, different power topologies as well as component selection can be used to achieve further power density reduction!

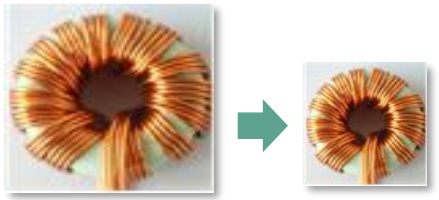
Infineon, a Silicon and WBG system technology provider

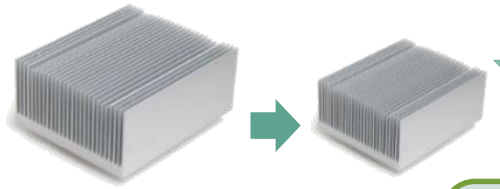




Benefits of Lower Switching Losses with SiC MOSFETs







Reduced control design effort & fewer gate drivers

Simplified topology due to low switching losses

SiC

Higher switching frequencies

smaller magnetics & lower losses

Higher efficiency due to lower losses

Smaller heatsink & packaging

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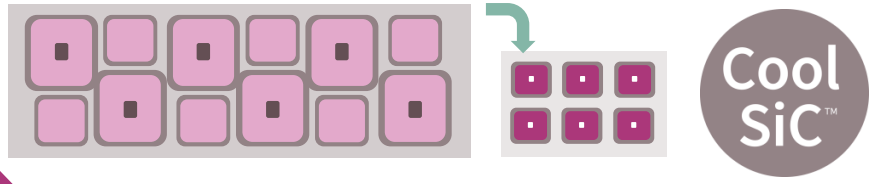
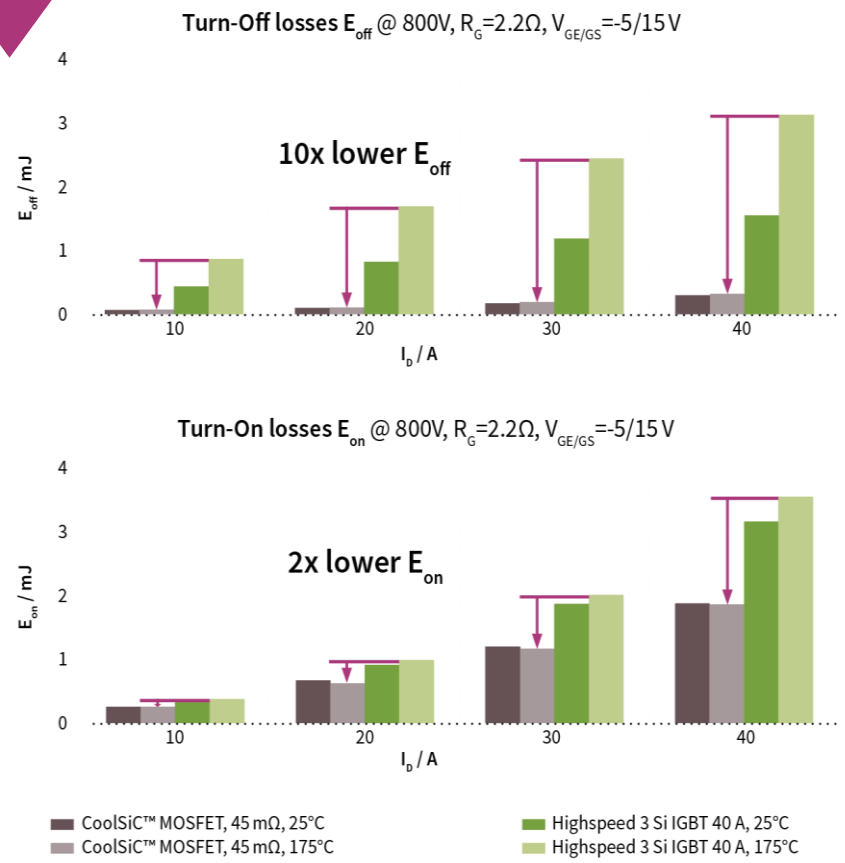
SiC MOSFETs – what differentiates them from IGBTs?

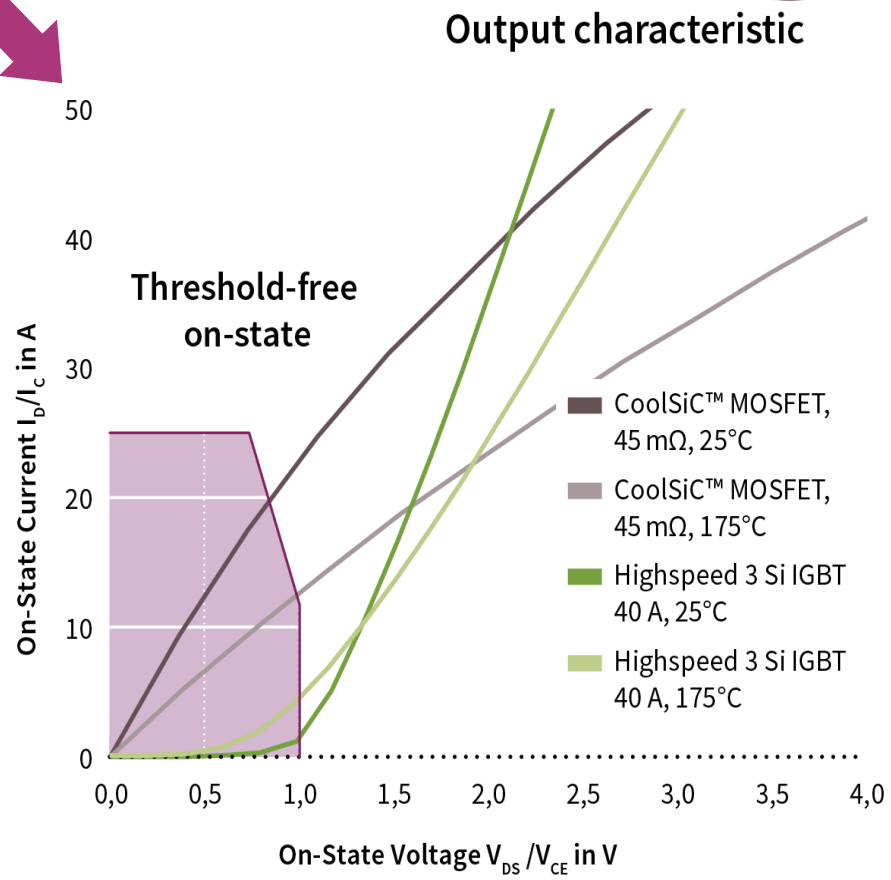
Benchmark in switching losses

Integrated freewheeling diode

Knee voltage free on-state







Losses per kHz for a 100A Si IGBT and SiC MOSFET at Same Current Level

Maximum Junction Temperature	
Switch	100.5°C
Diode	100.5°C
Switching Losses	
Switch	0.6W
Diode	0W
Conduction Losses	
Switch	13.3W
Diode	2.6W
Total Losses	
Switch	13.8W
Diode	2.6W

FF11MR12W1M1_B11

SiC MOSFET

Switching loss

At 1 kHz is 4% of total loss

Maximum Junction Temperature	
Switch	116.7°C
Diode	99.2°C
Switching Losses	
Switch	6.0W
Diode	1.4W
Conduction Losses	
Switch	27.0W
Diode	5.4W
Total Losses	
Switch	33.0W
Diode	6.8W

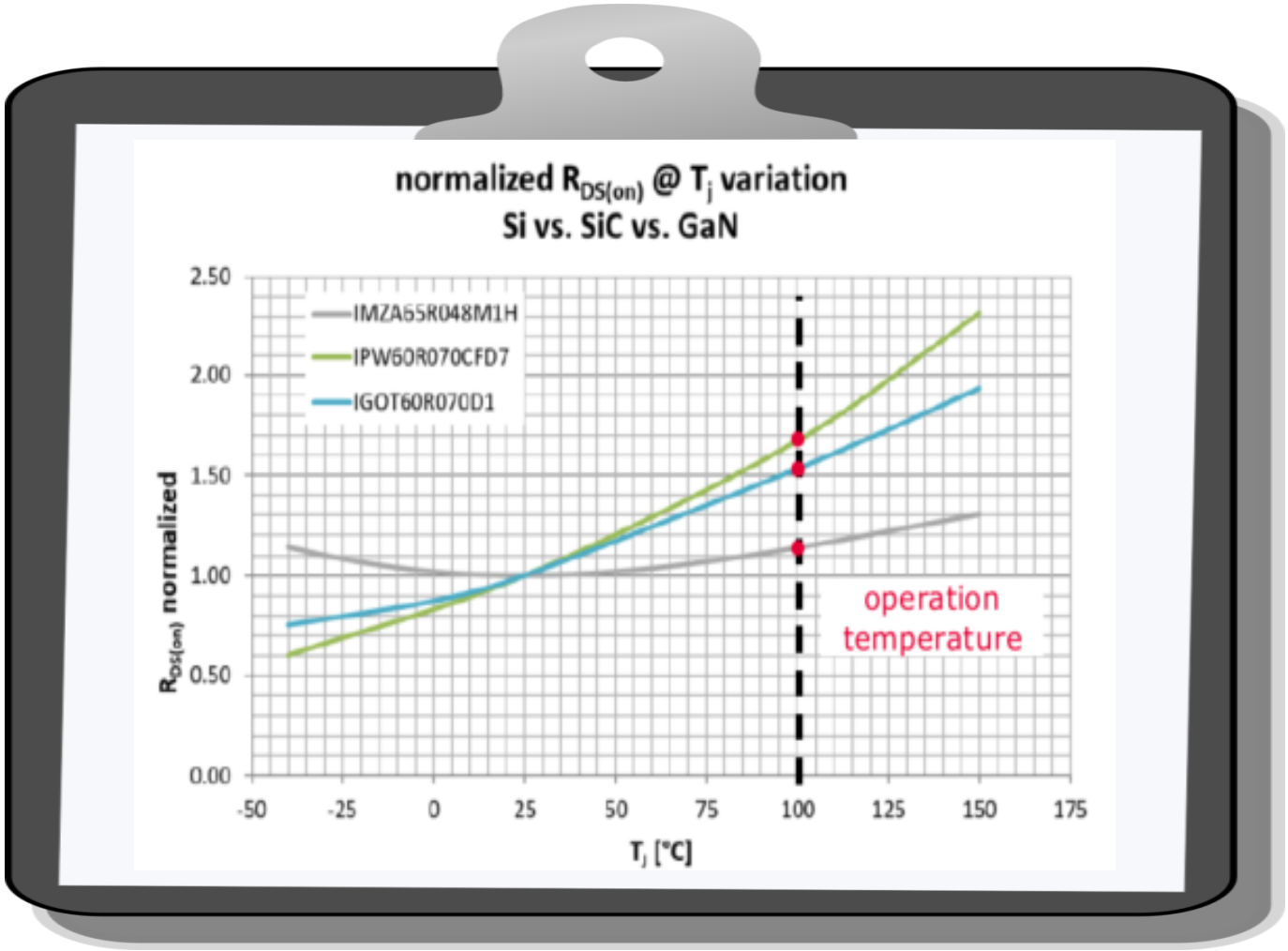
FS100R12W2T7

IGBT

Switching loss

At 1 kHz is 19% of total loss

$R_{DS(on)}$ over junction temperature (normalized)



› Considering the thermal behavior of the $R_{DS(on)}$, CoolSiC™ shows the best performance as the $R_{DS(on)}$ increase over the T_J is much smaller

› Multiplication factor kappa (k) of the typical $R_{DS(on)}$ for hot operation:

Operation temperature T_J = 100 °C

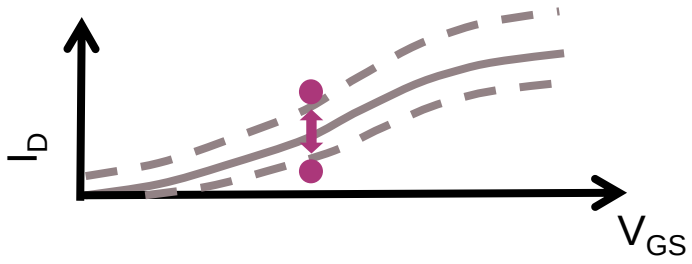
CoolMOS™ → **k = 1.67**

CoolSiC™ → **k = 1.14**

CoolGaN™ → **k = 1.53**

A practical example of a CoolSiC™-based EV Charger design

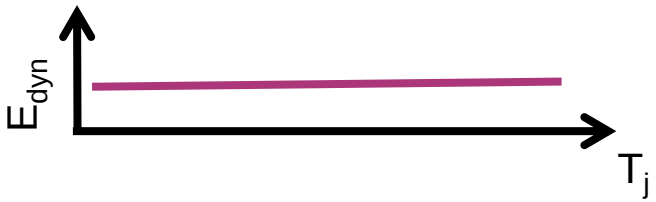
“Softer” transconductance



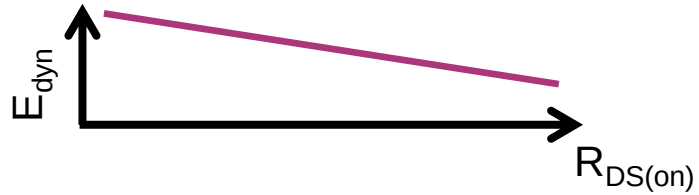
Larger increase in RDS(on) with temperature so a strong positive feedback

Paralleling CoolSiC™ devices

Slight increase in switching losses due to temperature



Correlation that higher RDS(on) parts have lower switching losses



Paralleling Devices to Reduce Conduction Losses

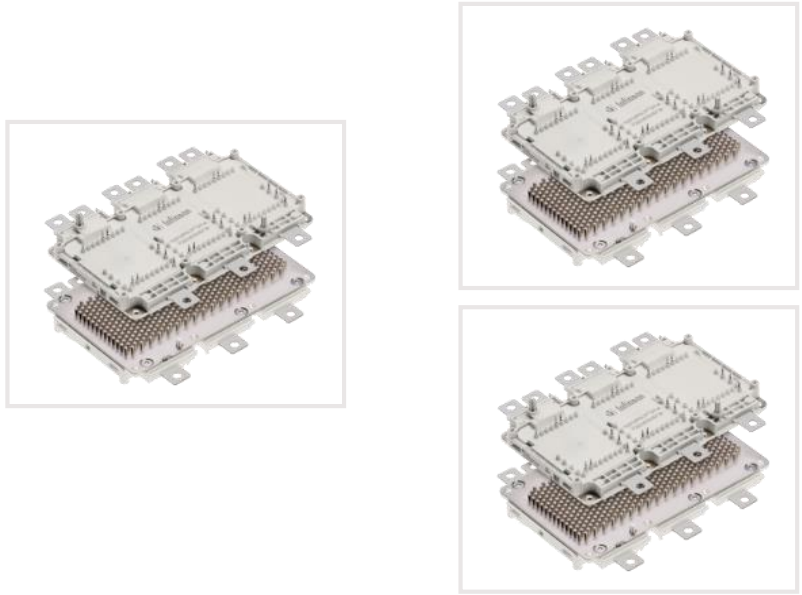
› Conduction Losses IGBT
› 1 module 2 modules

≈ 30% reduction

Conduction Losses SiC MOSFET

1 module 2 modules

≈ 60% reduction



Note loss reduction >50% due to reduced T_j

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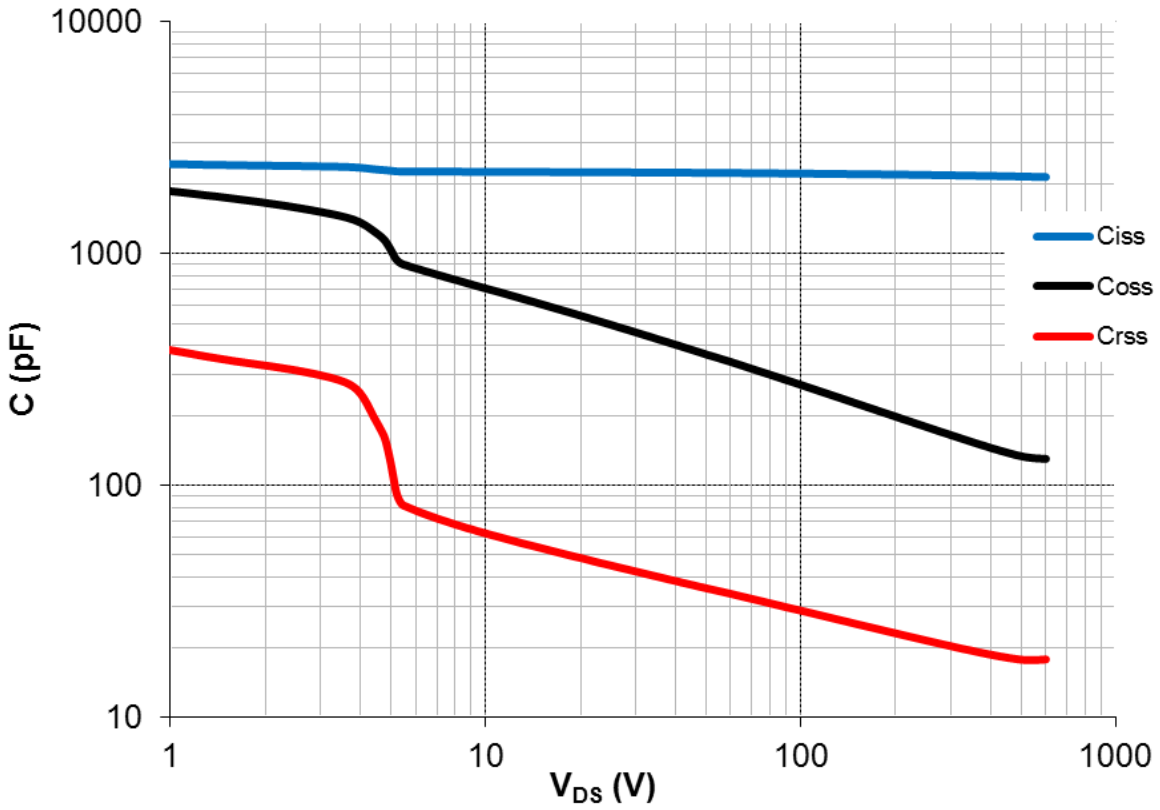
CoolSiC™ MOSFET suitable for ZVS operation

Device capacitances at 1 MHz, V_{GS} = 0



- C_{iss} >> C_{oss} >> C_{rss}
- Small C_{rss} (~10 smaller than C_{oss})

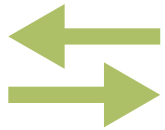
Well suited to suppress parasitic re-turn-on (PTO)

Low C_{oss} allows a fast VDS transition at turn-on

CoolSiC™ in DC EV charging
Optimal figure of merit for each charging design stage

RDS(on)* Qoss

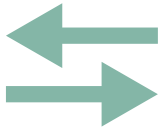
› Facilitates dead time / resonant current settings and enables higher frequency



ZVS type DC-DC converter

RDS(on)* Qrr

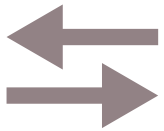
› Enables applications with repetitive hard commutation on the body diode



PFC type AC-DC converter

RDS(on)* Qg

› Reducing driving losses especially in light load conditions



Light load efficiency

Why performance increase leads to challenges?
Comparing devices @ 50 A, 20 kHz and above

		2xIKW40N120H3	FF23MR12W1M1_B11
dv/dt	kV/µs	25	100
di/dt	kA/µs	4	11
Gate drive	V	0/15	-2/15
Gate charge	µC	0.37	0.12
Total gate resistor	Ohm	12	3.0
Total switching losses	mJ	8	0.65
Gate peak current	A	2.5	5.7
Charge/peak current	ns	150	21
Driver losses	W	0.11	0.04
Driver losses @ increased fs (5x)	W	n/a	0.2

Faster transients

Increased gate peak current

Faster gate charging

Drive power

Why performance increase leads to challenges?
Impact of faster transients

$$U = L * dildt$$

- DC-link stray inductance
  → Overvoltage
  11 kA/µs * 10 nH = 110 V
- Common source side inductance
  → Negative feedback
  11 kA/µs * 0.5 nH = 5.5 V
- Insertion impedance of a current probe
  → Slowing down switching

$$I = C * dvldt$$

- Driver supply stray capacitance
  → Injecting current
  100 kV/µs * 15 pF = 1.5 A
- Overlap of two layers in PCB
  5 cm² with 250 µm distance
  → Injecting current
  100 kV/µs * 78 pF = 7.8 A
- Wrong drive signals due to exceeding drivers common mode immunity
- Additional stress in isolation

Driving CoolSiC™ MOSFET
Information from the datasheet

Gate-Source Spannung Gate-source voltage			V_{GSS}	-10 / 20			V

Charakteristische Werte / Characteristic Values

				min.	typ.	max.	
Einschaltwiderstand Drain-source on resistance	I_D = 50 A V_{GS} = 15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$R_{DS\,on}$		22,5 29,5 33,0		mΩ
Gate-Schwellenspannung Gate threshold voltage	I_D = 20,0 mA, V_{DS} = V_{GS}, T_{vj} = 25°C (tested after 1ms pulse at V_{GS} = +20 V)		$V_{GS(th)}$	3,45	4,50	5,55	V
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_D = 50 A, V_{DS} = 600 V, Lσ = 35 nH di/dt = 11,0 kA/µs (T_{vj} = 150°C) V_{GS} = -5 V / 15 V, R_{Gon} = 1,00 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		0,49 0,535 0,559		mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_D = 50 A, V_{DS} = 600 V, Lσ = 35 nH du/dt = 53,0 kV/µs (T_{vj} = 150°C) V_{GS} = -5 V / 15 V, R_{Goff} = 1,00 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		0,094 0,094 0,091		mJ
Kurzschlußverhalten SC data	V_{GS} = -5 V / 15 V, V_{DD} = 800 V V_{DSmax} = V_{DSS} -L_{sDS} ·di/dt R_G = 10,0 Ω	t_P ≤ 2 µs, T_{vj} = 25°C t_P ≤ 2 µs, T_{vj} = 150°C	I_{SC}		420 410		A A

Important note: The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN 2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

This is the voltage to test and specify $R_{DS(on)}$

Exceeding this might cause immediate destruction

Threshold voltage indicates if turn-off with 0 V might be feasible

For this voltage, SC is specified

This AN provides information on impact of gate voltage on degradation

But which conclusion do we draw out of this?

Mapping drive voltage to applications

Application	Positive	Negative
Discrete, no SC requirement	15 V – 18 V	0 V
Discrete, SC requirement	15 V	0 V
Module, drive application (limited speed, SC)	15 V	0 V
Module, fast application	15 V – 18 V	-2 V – 4 V
2nd source application	15 V – 18 V	... -5 V

Drive voltage range close to IGBT enables

- Use of established driver ICs and power supplies
- Easy use of IGBT and CoolSiC™ in the same system

Designing a SiC MOSFET like this does not impair performance!

Driving CoolSiC™ MOSFET
Driver output stage requirement

Output peak current

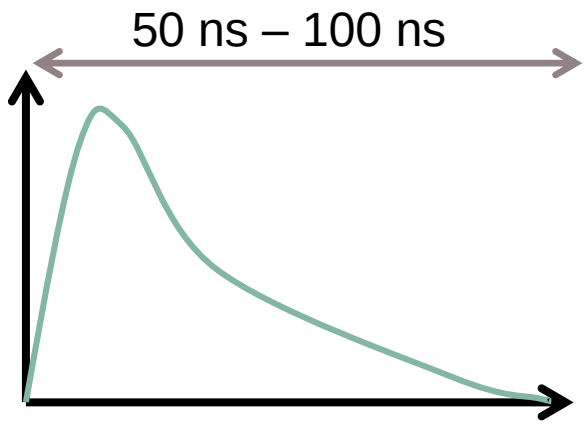
$$I_G = \frac{V_{tot}}{R_G + R_{Gint}}$$

This overestimates required peak current by ignoring:

- Output impedance
- Gate inductance

→ Minimum rating of driver with some margin required

Rise time



Driver output rise time should not slow down gate current rise

- Target 10 ns – 15 ns (for example here)

Power

$$P_{Dr} = f_s * V_{tot} * Q_G$$

Q_G is a function of V_{tot}

- See diagram in datasheet

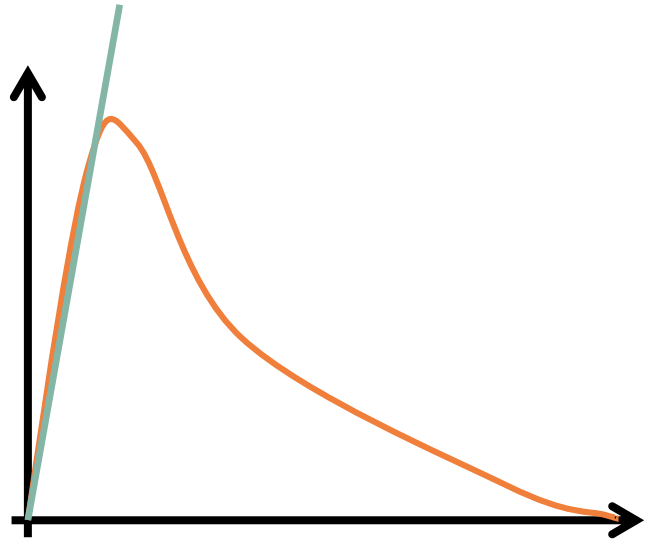
P_{Dr} is dissipated in:

- Driver IC
- R_G
- R_{Gint}

Risk of overheating with insufficient output stage

Driving CoolSiC™ MOSFET
Layout considerations

Also here the required gate current governs design



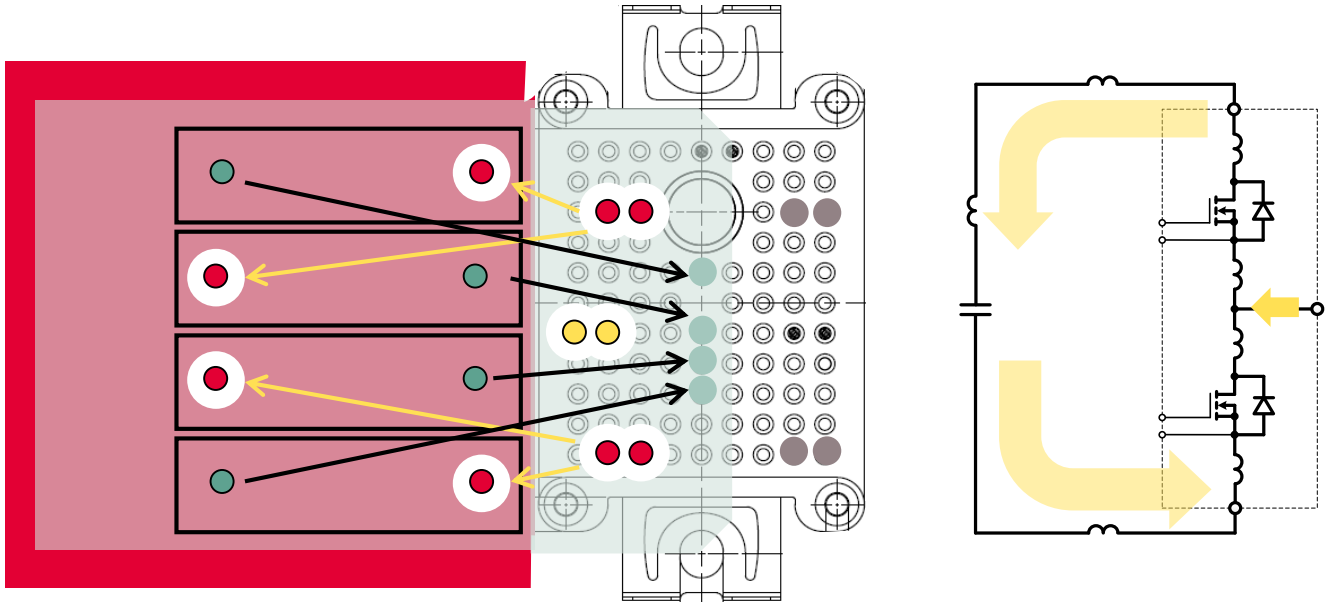
Too high gate inductance will limit di/dt or even cause oscillation

Target (example): 50 nH

Within the PCB

- Stripline approach is best
- Same methods apply as for DC-link
- Distance between layers can be smaller
- Routing in same layer side by side reduces some performance

Current Flow in Both PCB DC Bus Layers



- Short current paths, small current loops, multiple paths in parallel
- If possible, current flowing in opposite planes

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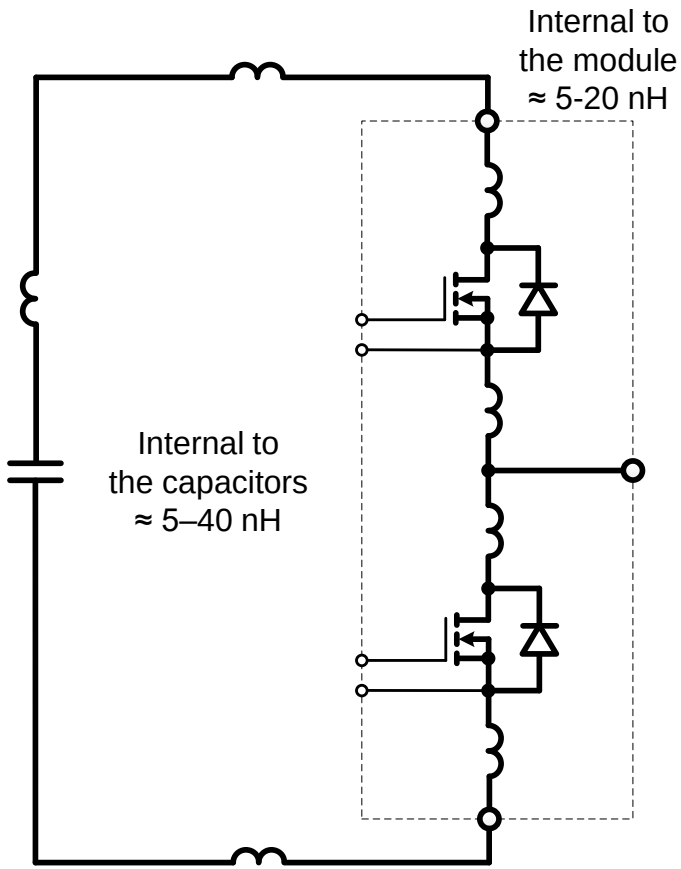
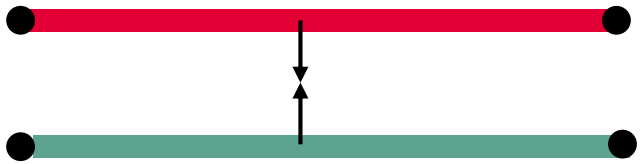
Where is the System Inductance and How to Reduce it?



Overlapping go
and return paths

Wide flat planes with multiple
connection points



Keep loops as
small as possible

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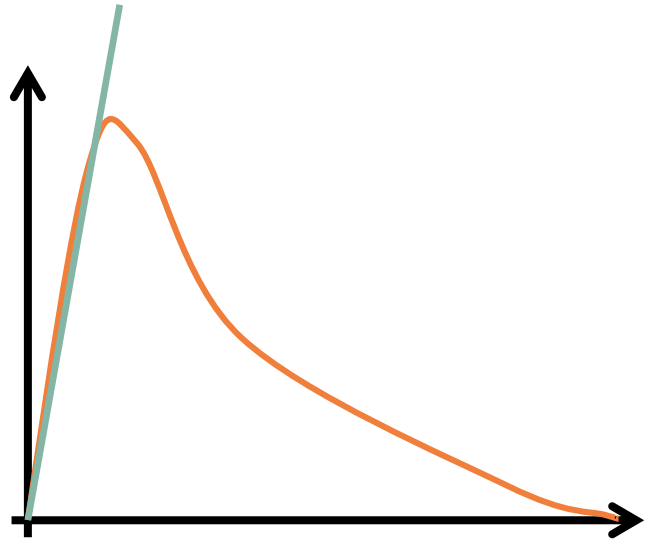
Driving CoolSiC™ MOSFET
Layout considerations

Also here the required gate current governs design



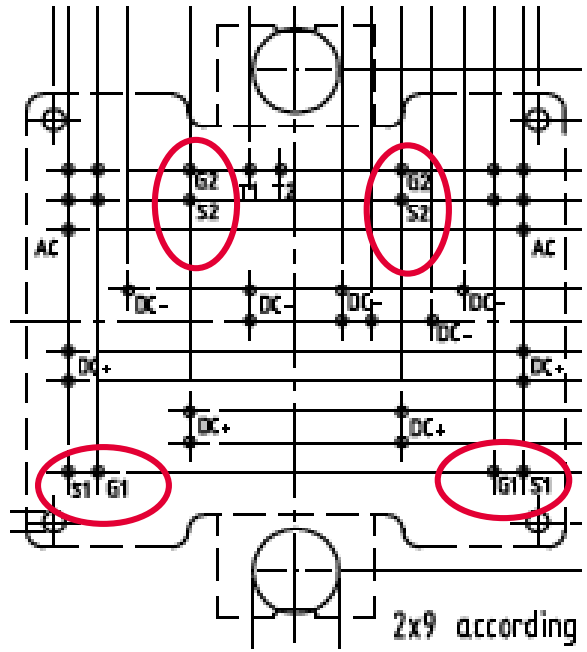
Too high gate inductance will limit di/dt or even cause oscillation

Target (example): 50 nH

Board-to-board or board-to-module

Use multiple pins in parallel

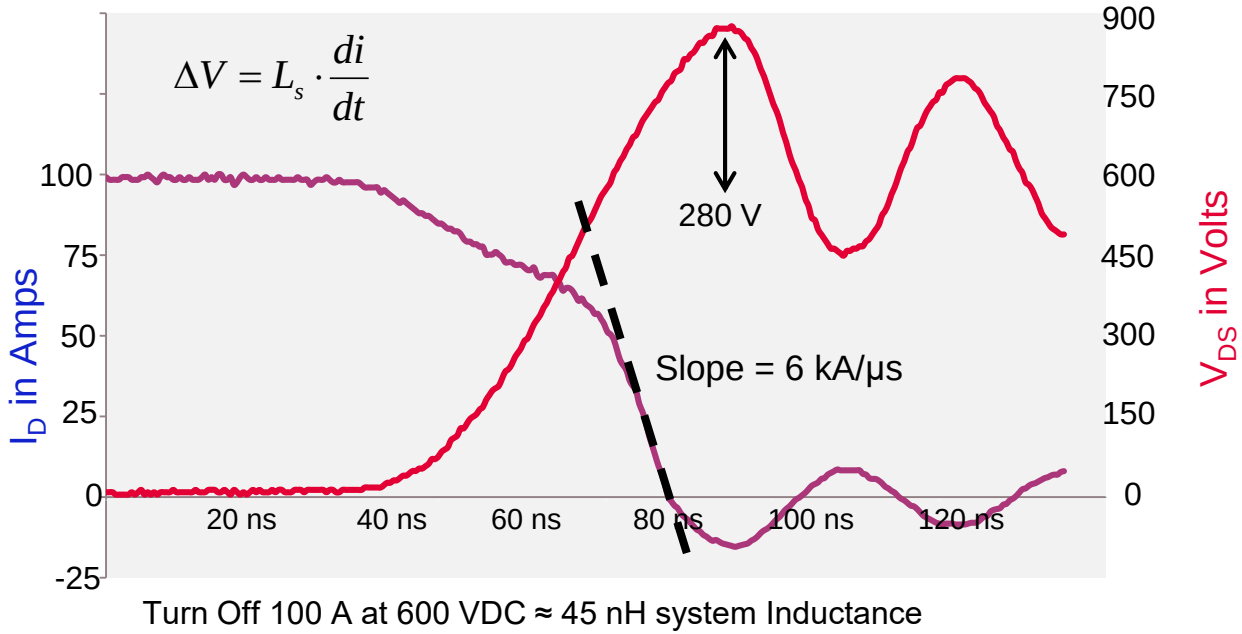
Example: FF in Easy 2B



How to Reduce Voltage Overshoots and Oscillations at Turn Off

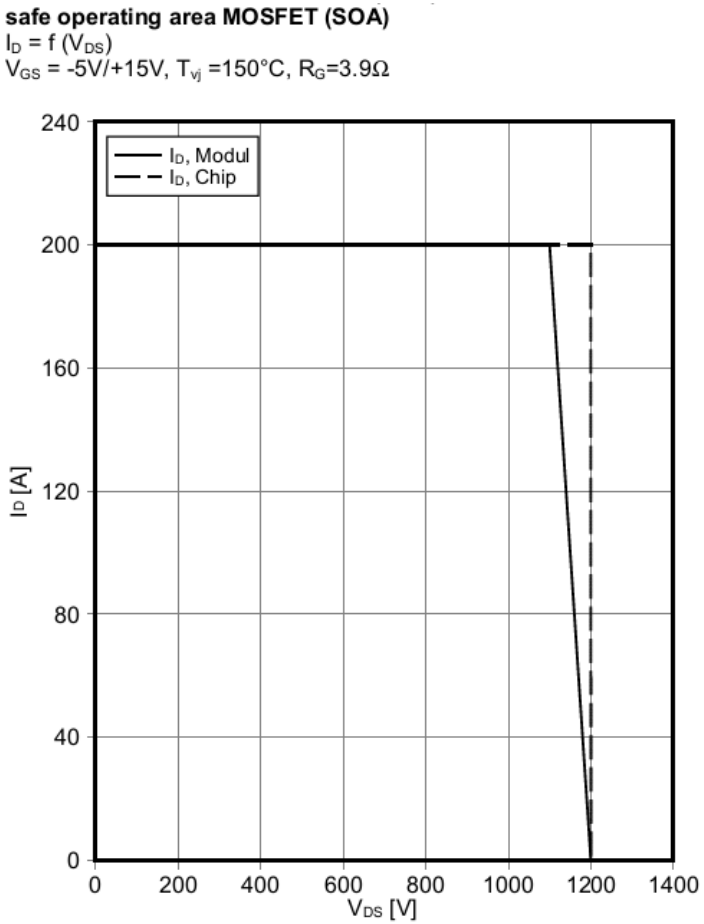
- Reduce the di/dt level
- Reduce the loop inductance

Voltage Over-shoots and RBSOA



Turn Off 100 A at 600 VDC ≈ 45 nH system Inductance

Typical SOA curve for a 100A 1200V SiC MOSFET module



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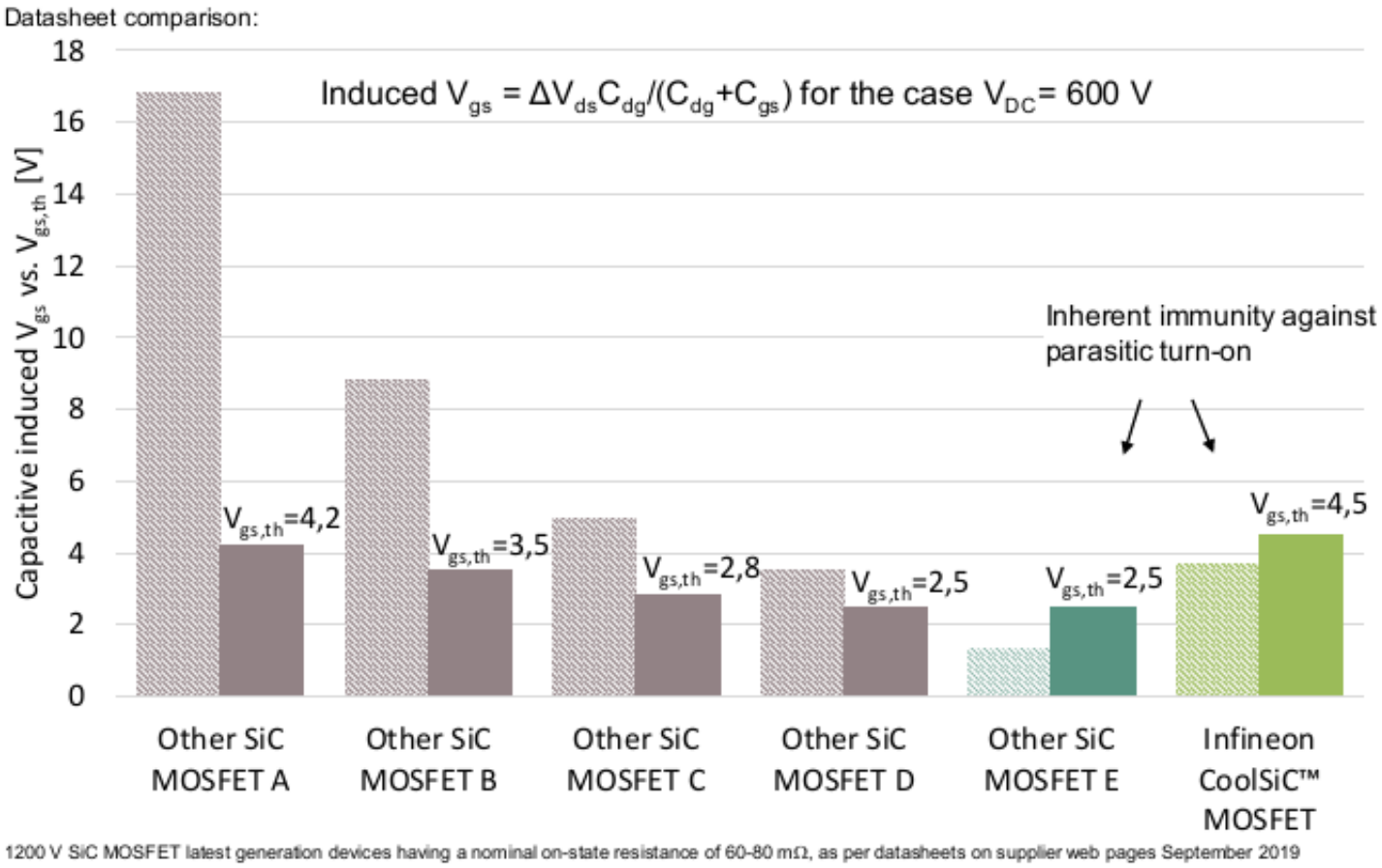
Driving CoolSiC™ MOSFET
Avoiding parasitic turn-on

By device design



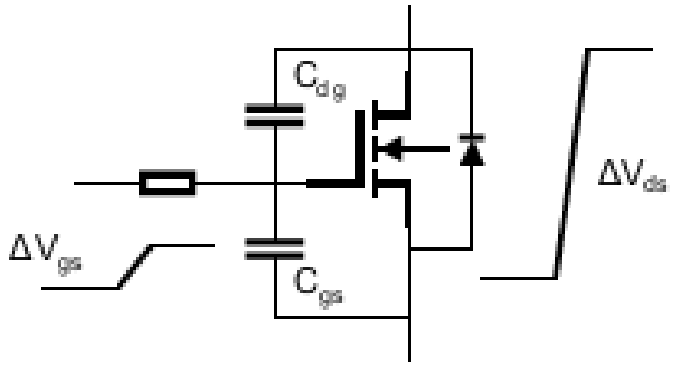
1200 V SiC MOSFET latest generation devices having a nominal on-state resistance of 60-80 mΩ, as per datasheets on supplier web pages September 2019

Negative gate voltage

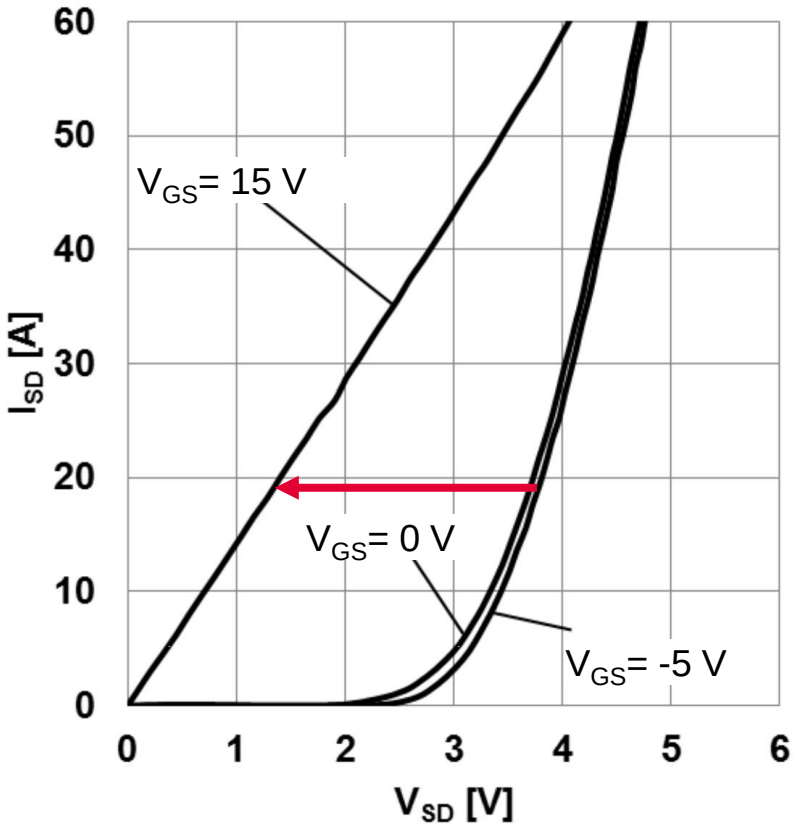
- Additional margin
- For modules in fast switching applications

Active Miller Clamp

- Bypass R_{Goff}
- Gain margin for 0 V/15 V driving



Synchronous rectification



Typical body diode forward current as function of forward voltage, VGS as parameter (I_{SD}= f(V_{SD}), T_{vj}= 175ºC, t_P= 20 µs)

Body diode forward voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 20 A T_{vj} = 25ºC T_{vj} = 100ºC T_{vj} = 175ºC	- - -	4,1 4,0 3,9	5,2 - -	V

What does synchronous rectification mean?

Moving operating point from diode characteristic to resistive line by applying positive gate bias

How can this be achieved?

Complementary signals for a half-bridge

This is the standard method for gating half-bridges

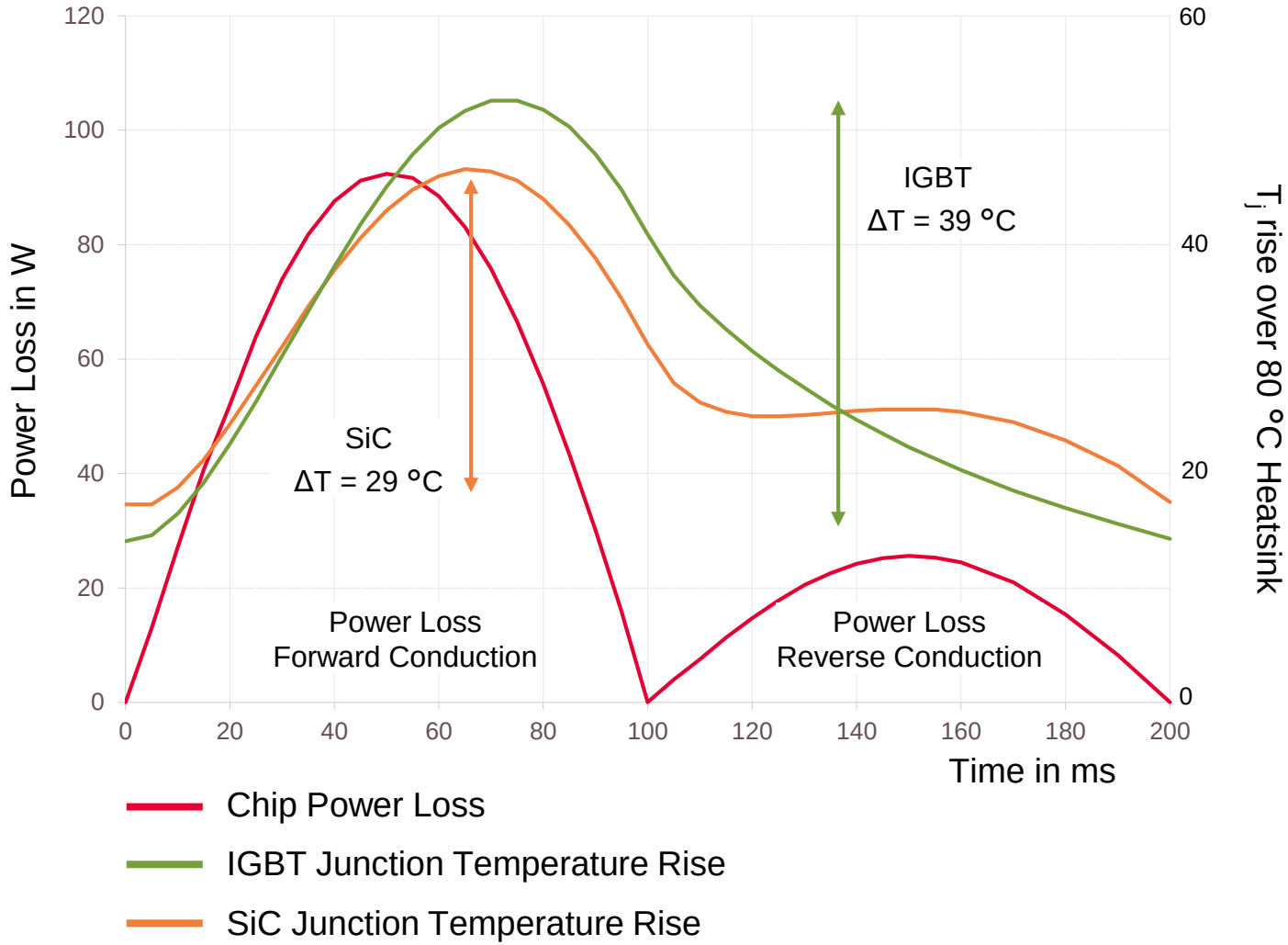
Deadtime should be minimized

SC protection for CoolSiC™
Challenges for implementation

Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_D = 25 A, V_{DS} = 600 V, L_σ = 30 nH du/dt = 41.6 kV/µs (T_{vj} = 150ºC) V_{GS} = -5 V/15 V, R_{Goff} = 1.00 Ω	T_{vj} = 25ºC T_{vj} = 125ºC T_{vj} = 150ºC	E_{off}	0.033 0.035 0.035	mJ
Kurzschlußverhalten SC data	V_{GS} = -5 V/15 V, V_{DD} = 800 V V_{DSmax} = V_{DSS} - L_{sDS} di/dt R_G = 10.0 Ω	t_P ≤2 µs, T_{vj} = 25ºC t_P ≤2 µs, T_{vj} = 150ºC	I_{SC}	210 205	A A

- >8 x $I_{D\ nom}$ in 45% of the active area of an IGBT
- SC is specified in the datasheet
  → Need to account for degradation
- Our limit of 2 µs for module or 3 µs for discrete already considers this!

Ripple Temperature at 5 Hz Operation IGBT & SiC MOSFET



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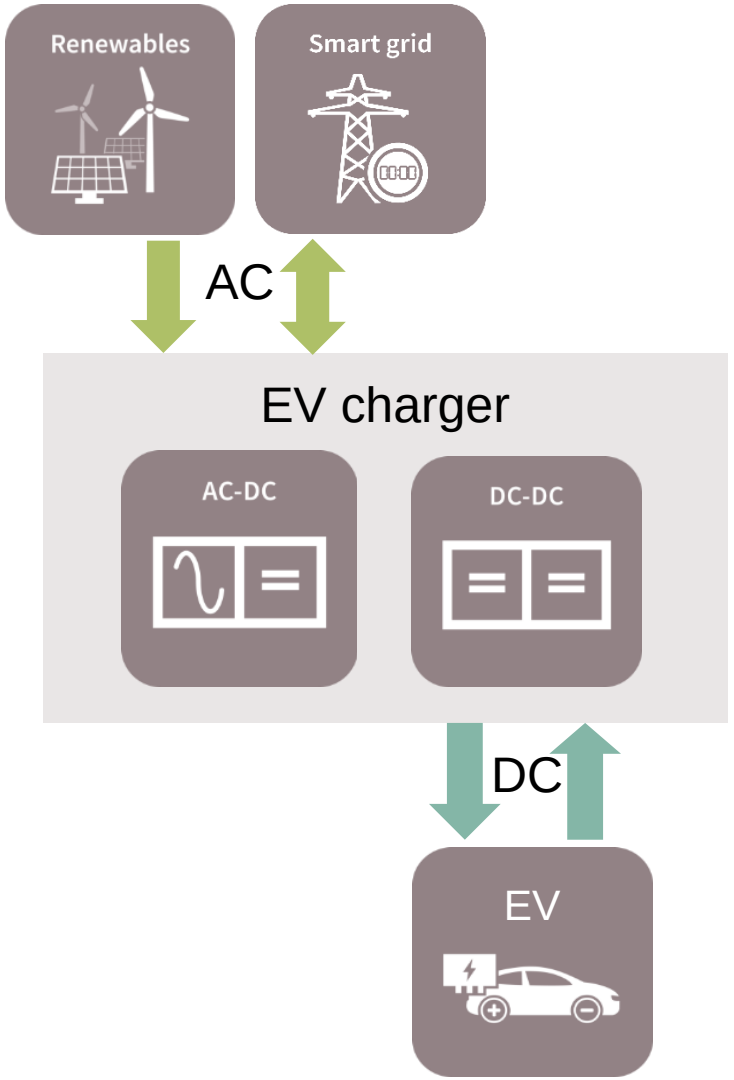
Why bi-directional EV charger solutions are becoming important



Bi-directional EV chargers enable:

- reverse energy flow from the EV to the grid / home / storage system
- new charging business models like V2B or V2G

Vehicle to Building (V2B)	Vehicle to Grid (V2G)
Combination with solar and energy storage systems	Peak load levelling Buffer for renewables

Key benefits of the modular subunit reference design concept

For developers

Less R&D times and efforts through universal power conversion approach

Flexible thermal management allows both air and liquid cooled systems

Versatile power control card with automotive grade microcontroller

Software for power control with user-friendly interface and options

For installers and operators

Wide DC output voltage range of **200 to 920 V** complies with all relevant EV charging standards and battery types

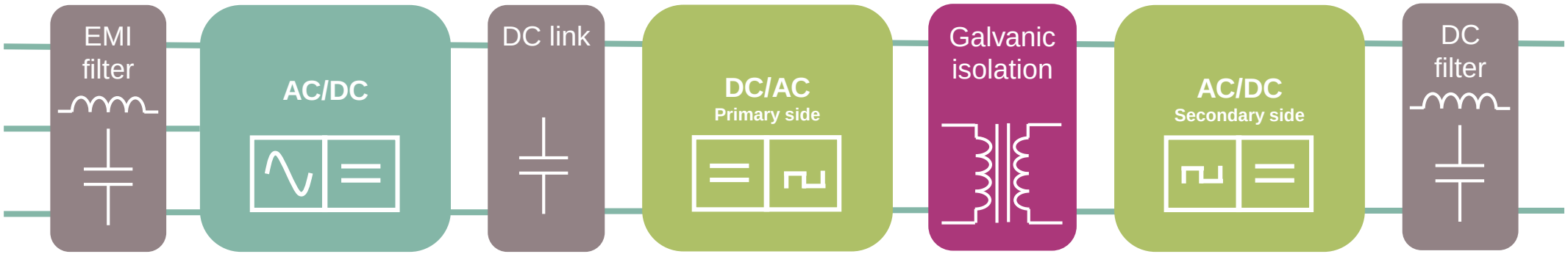
High power conversion efficiency saves energy and cooling efforts

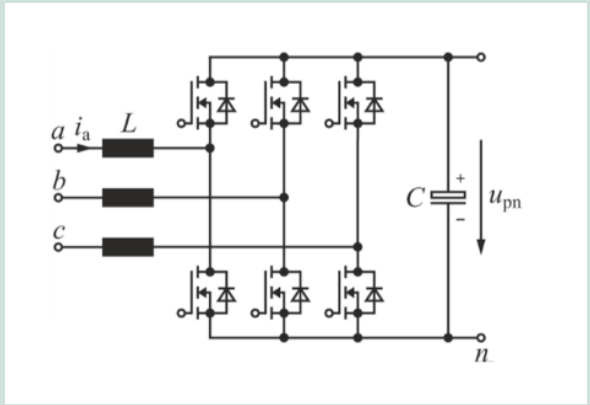
Bi-directional power flow capability enables new business models

Modular and stackable subunit to realize various high power chargers

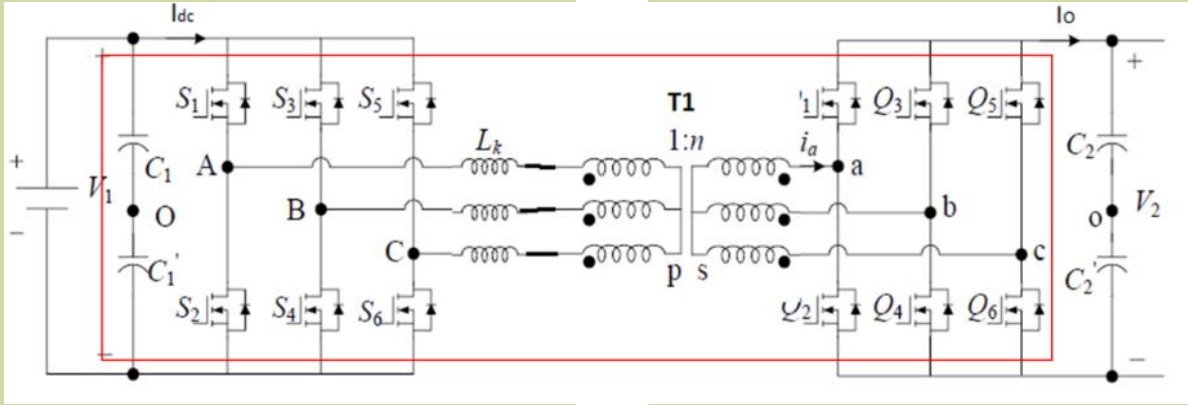
Reference design for subunits with up to 30 kW will use a 2-Level Active Front End PFC and a fully isolated Dual Active Bridge DCDC Converter

Power conversion topology





2-level Active Front End PFC

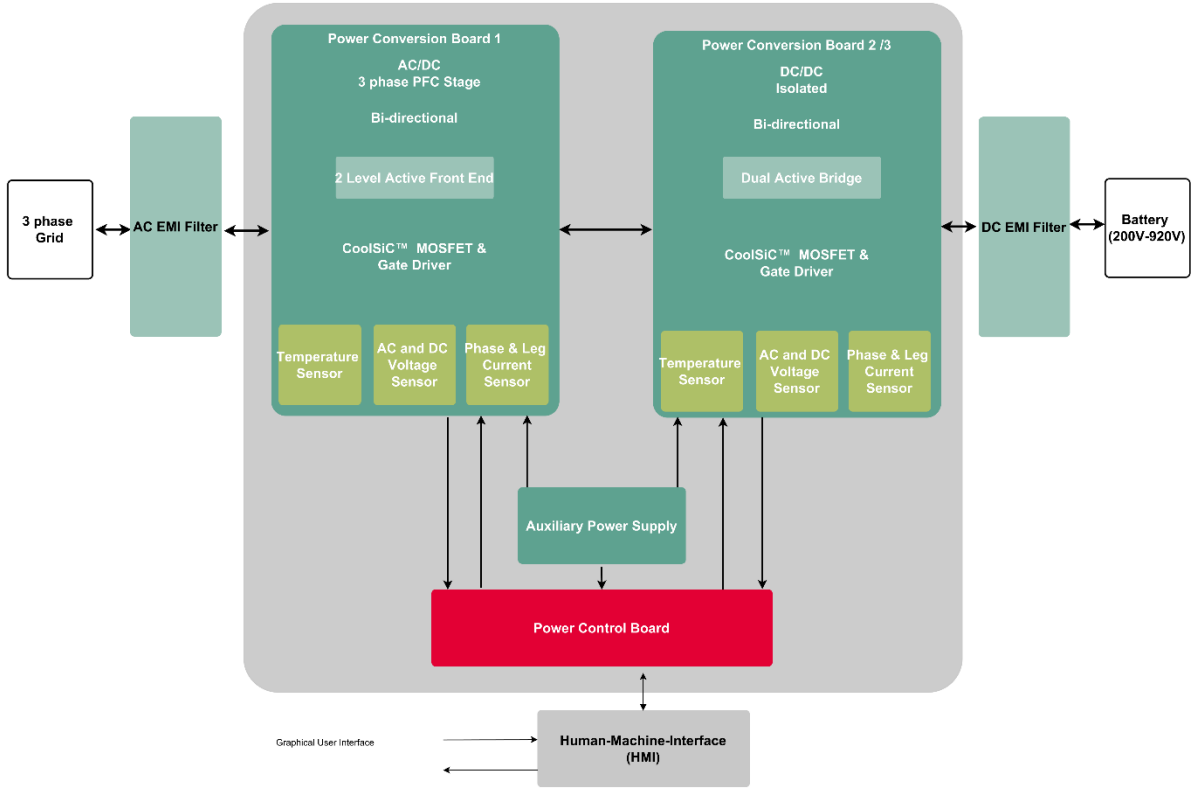


3-phase Dual Active Bridge
primary side

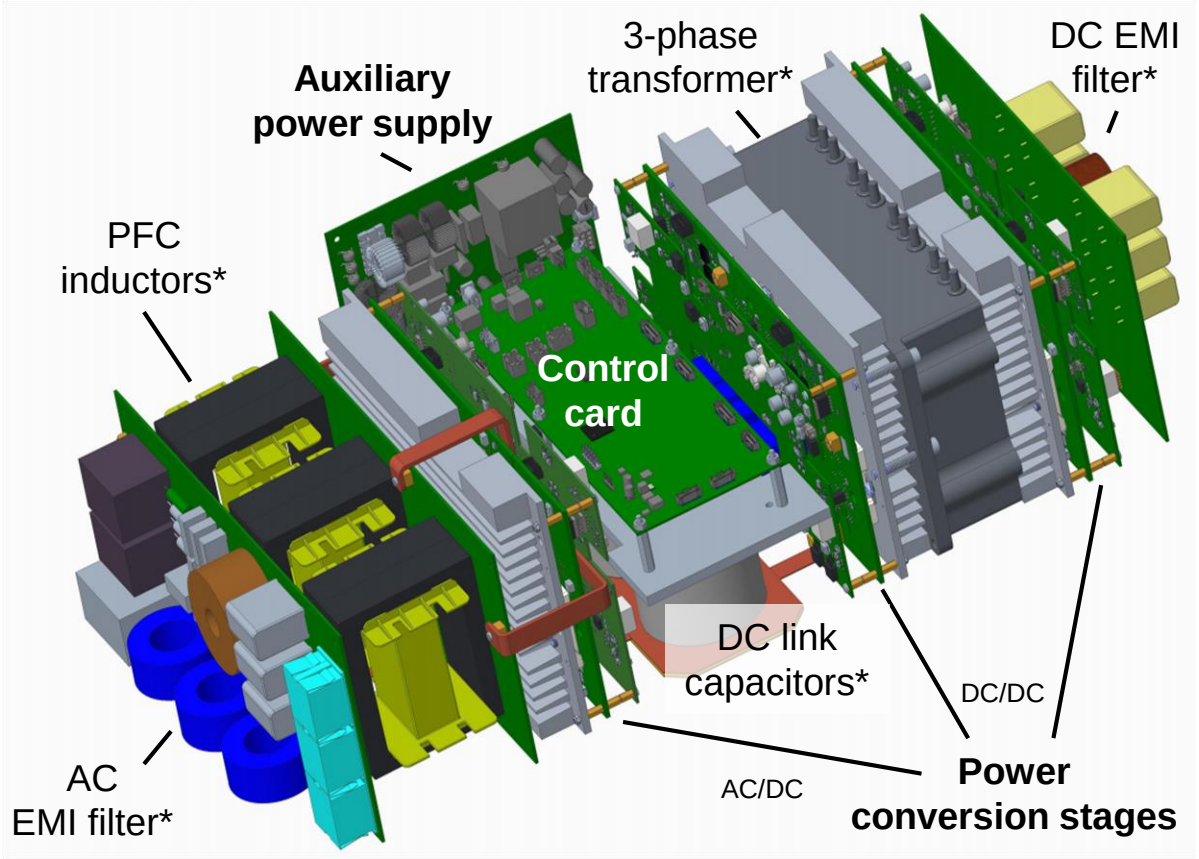
3-phase Dual Active Bridge
secondary side

The reference design concept considers all active and passive components needed to build a complete DC EV charger subunit

Block diagram



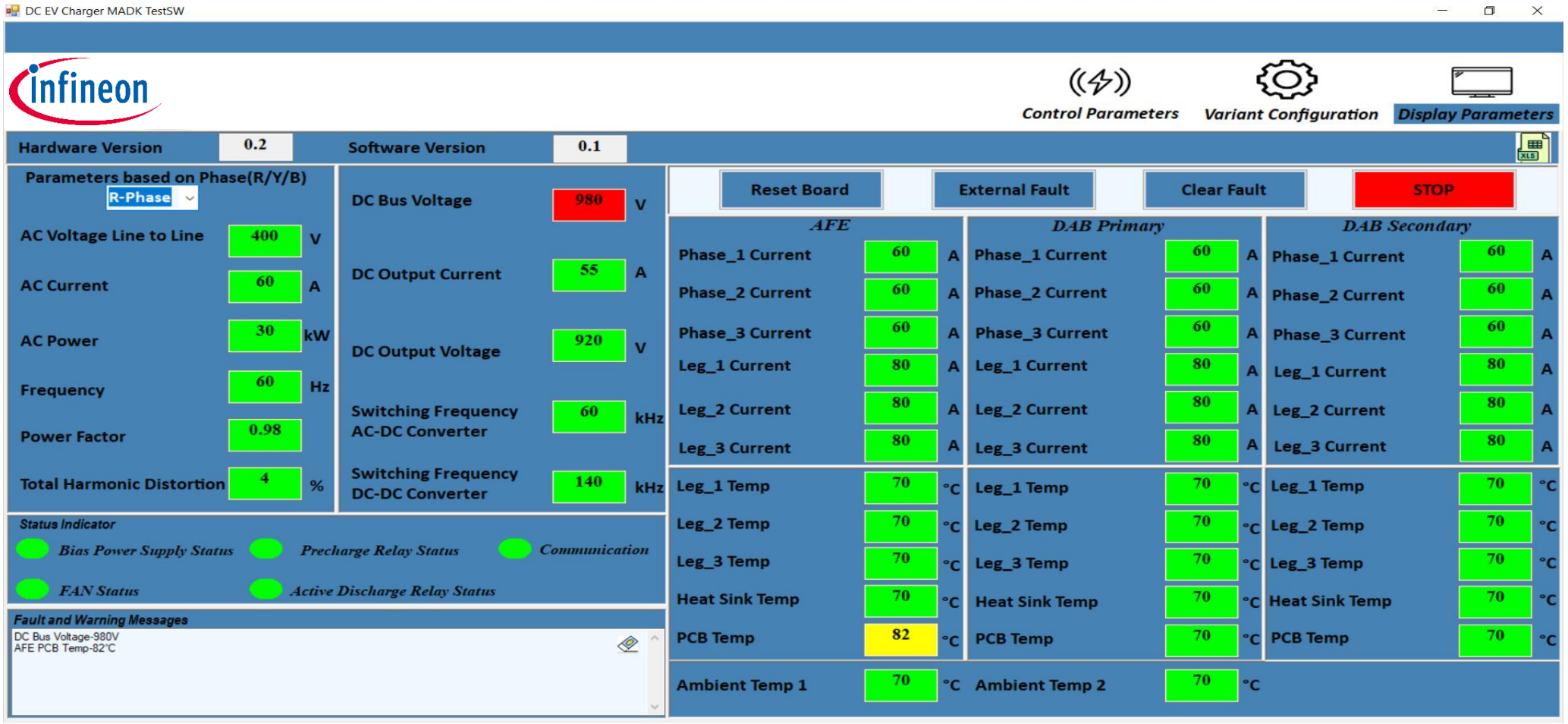
Subunit layout



* Passive components will not be offered by Infineon

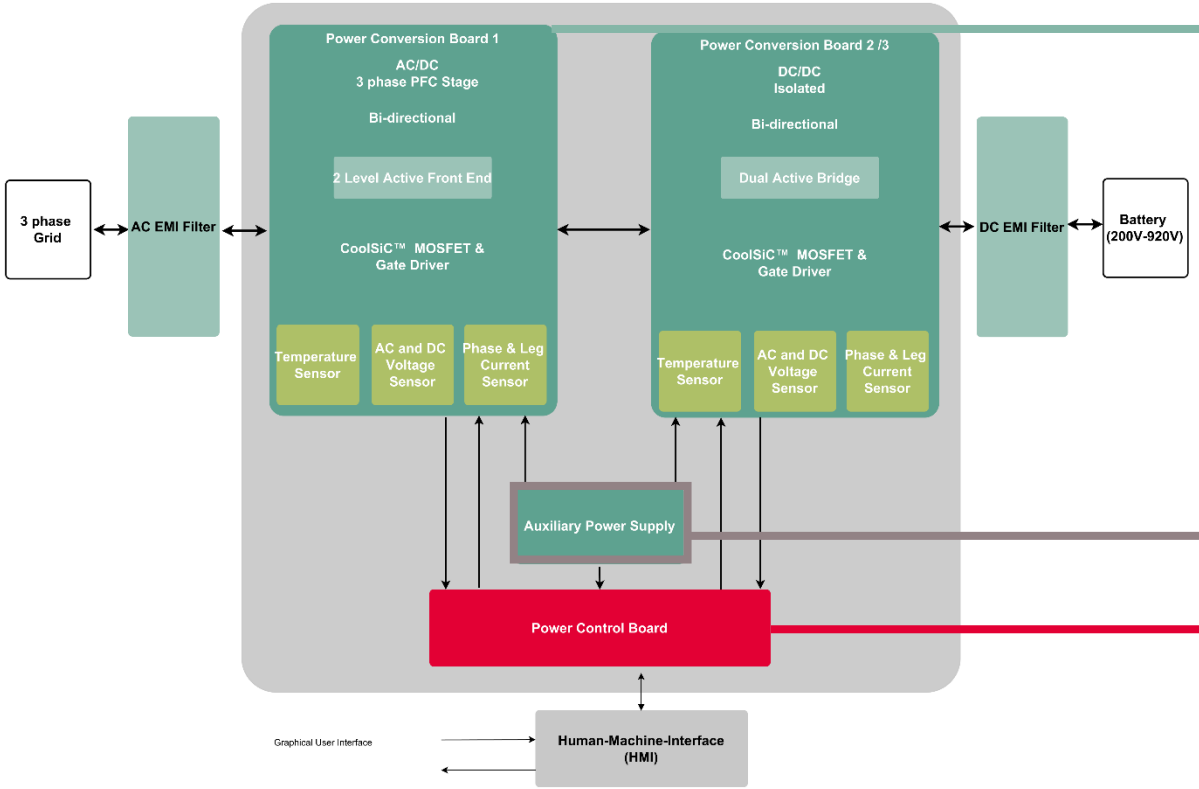
Control card will come with power control software and user-friendly GUI

GUI for power control software



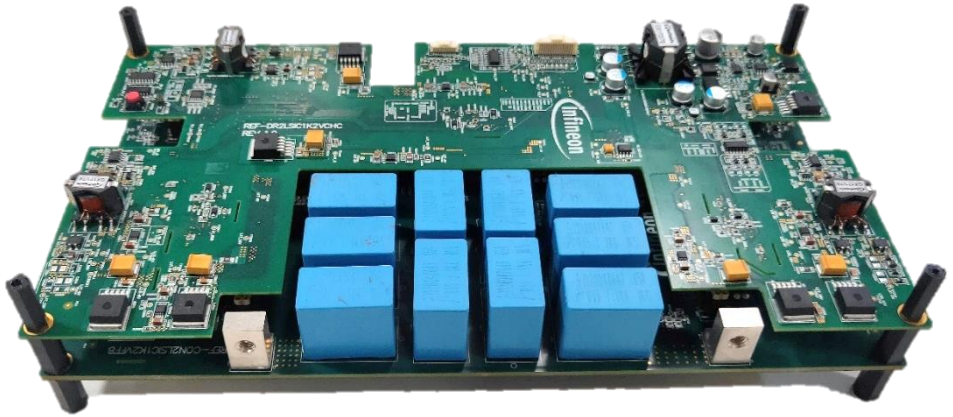
Infineon will offer fully assembled boards for all power conversion stages, a control card incl. software and aux power supply (planned for H1 2022)

Block diagram



Board layouts

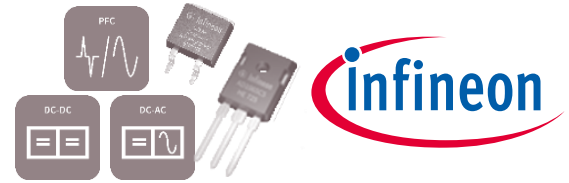
Power conversion boards:



Aux power supply:

Control board:

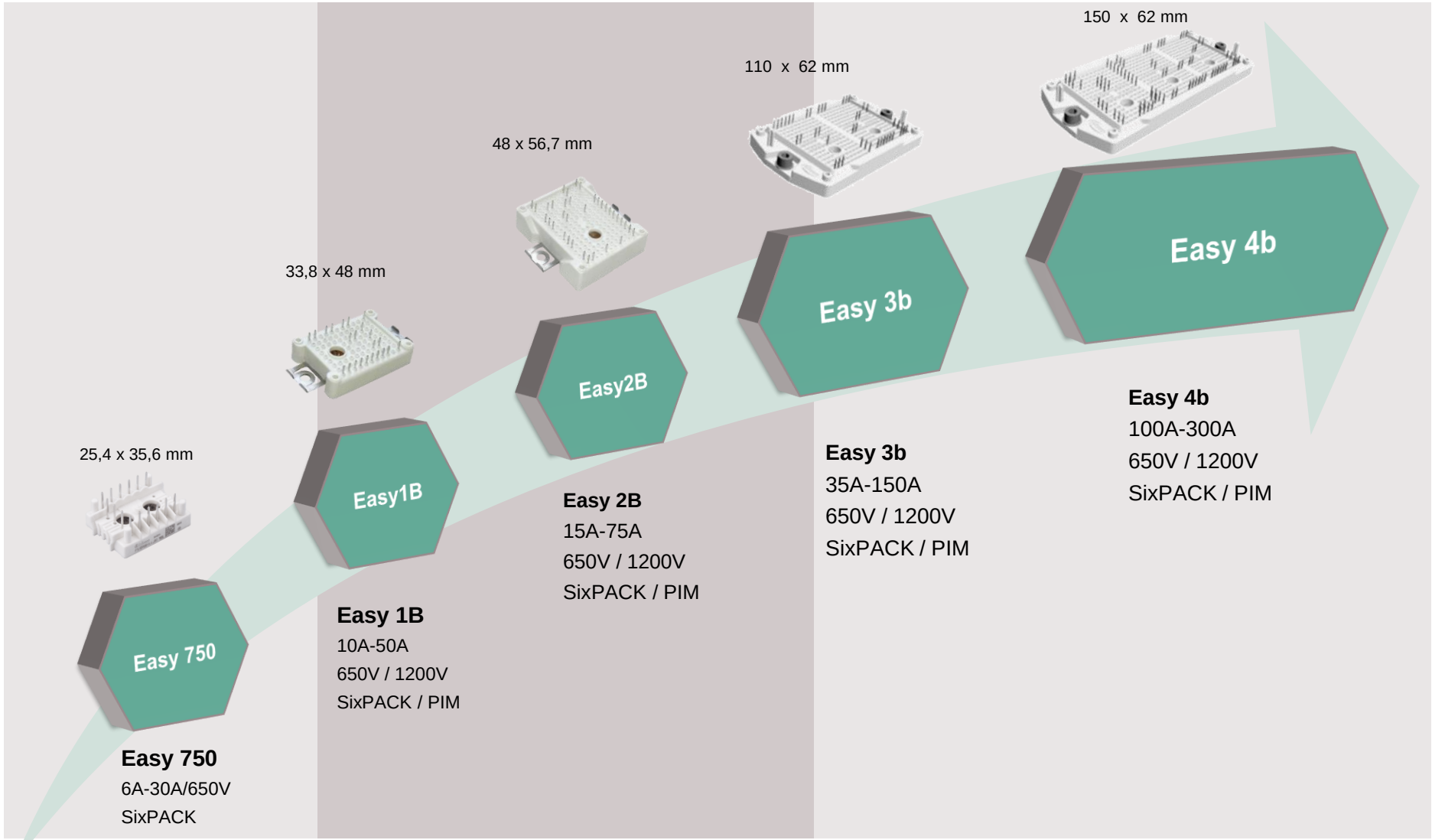
We continuously invest in HV Power Switch technologies



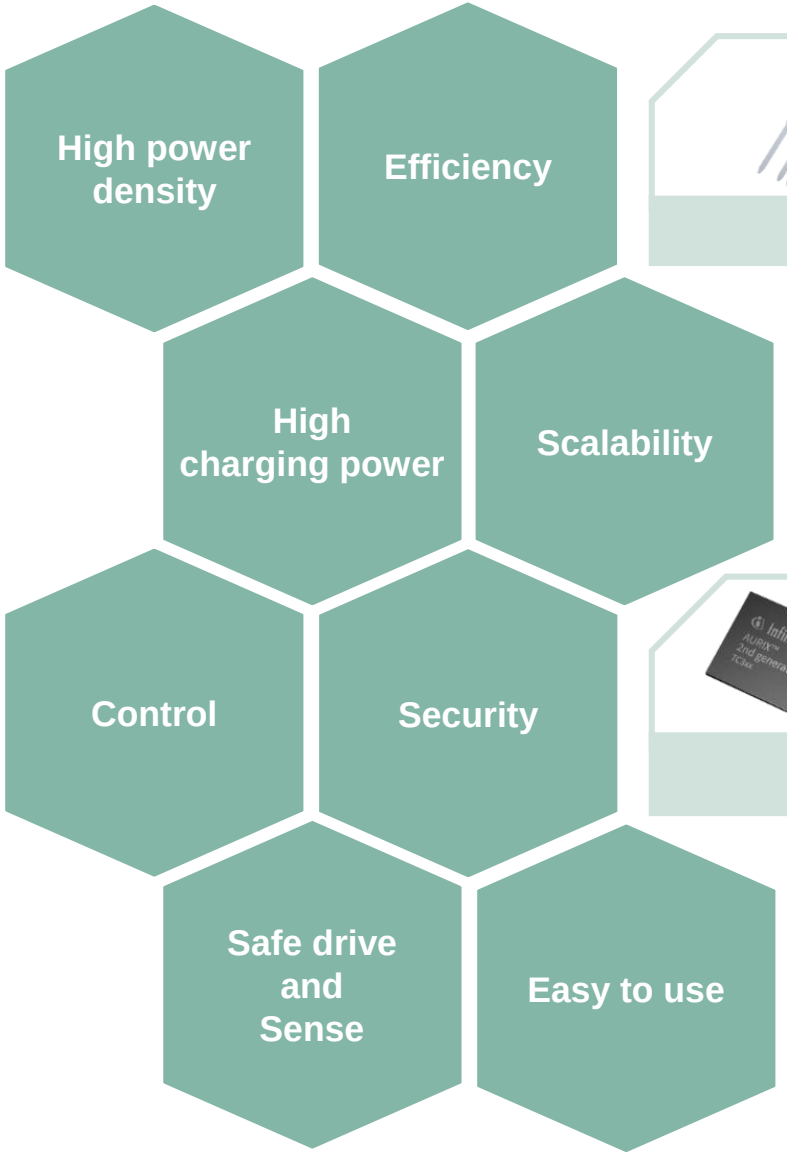
	2020	2021	>2022
HV CoolMOS™	**CoolMOS™ 650V CFD7** › TO263, TO263-7, TO220, TO247, › 18-230mΩ , various packages	**CFD7 QDPAK Extension** › High power density with TOP side Cooling	**CoolMOS™ next Gen** › Higher power density, lower switching losses › High thermal capabilities
650V CoolSiC™	**CoolSiC™ 650V Market launch** › TO263, TO263-7, TO220, TO247, › 18-230mΩ , various packages		**CoolSiC™ next Gen** › Lower Rdson variants › New packages, higher power dissipation capability
1200V CoolSiC™	**CoolSiC™ 1200V** › TO263, TO263-7, TO220, TO247, › 30-350mΩ , various packages	**CoolSiC™ 1200V Portfolio extension** › TOP Side Cooling , › <30mOhm for high power applications	**CoolSiC™ next Gen** › Lower Rdson variants › New packages, higher power dissipation capability
Gate Drivers	**Broad Portfolio for IGBT, SiC, MOS Power Switches** › Isolated, non isolated driver › Basic and reinforced types › Various channel and package config	**1EDN, 2EDN Portfolio extension** › Higher integration of external components › Support for new switching topologies (e.g. switching cap, etc)	

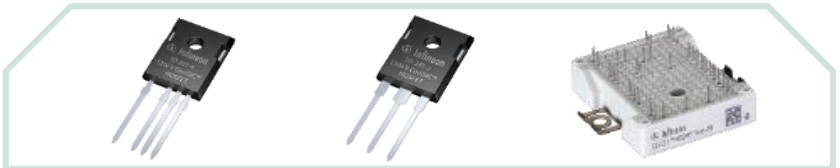
In Production *In Development* *Concept/Idea*

LMP Product Lineup: Easy Modules



Application trends are supported by Infineon's comprehensive DC charging ecosystem portfolio

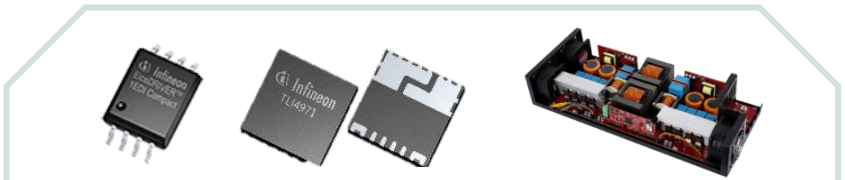




CoolMOS™ , IGBTs and CoolSiC™

Discrete components and modules like Easy and Econo family

AURIX™, XMC™, OPTIGA™



EiceDRIVER™, XENSIV™, Reference Designs

Supporting material for Infineon's EV charging offering

Application pages

- Fast EV Charging
- Chargers up to 150 kW
- Chargers from 50 kW to 350 kW

Collaterals and brochures

- Application presentation
- Application brochure
- Whitepaper
- Product brochure
- Product selection guide
- Product presentation
- Articles

Simulation tools

- IPOSIM

Evaluation boards

- Boards fast EV charging
- Boards chargers up to 150 kW
- Boards chargers from 50 kW to 350 kW

Videos / podcasts/ trainings

- Videos
- Podcast
- Trainings

Part of your life. Part of tomorrow.